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MANUAL
# of Operating & Maintenance
Procedures
for

Digital Multimeter
Model 3500

DATA PRECISION

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32-5003-E

MANUAL
# of Operating & Maintenance Procedures for

Digital Multimeter
Model 3500

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-.109724
DC
AC
kΩ
RATIO
.1
1
10
100
1K
10K(kΩ)
AUTO
DATA PRECISION
3500
POWER
R

Model 3500 Digital Multimeter

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Chapter 1

INTRODUCTION

The Model 3500 is a 5-1/2 digit wide-range digital multimeter, using improved second-generation features of the innovative Tri-Phasic^{TM} design first introduced by Data Precision in the Series 2500 Multimeters. The Model 3500 DMM provides a choice of either completely autoranging voltage measurements from 1 microvolt to 1 kilovolt and resistance down to a resolution of 1 milliohm, or direct manual range control.

The instrument features:

Tri-Phasic^{TM} A/D Conversion,
Iso Polar^{TM} Reference Generation, and
Ratiohmic^{TM} Resistance Measurements

1.1 TRI-PHASIC A/D CONVERSION CYCLE

The Tri-Phasic technique dramatically reduces three of the four major sources of error in conventional DVM circuits; zero offset and offset drift; resistance tolerance and drift; and ramp-time-constant tolerance and drift. In the first phase of operation, automatic zero-setting occurs. . . automatically updating an error-integrator/memory circuit, every conversion cycle. In the second phase, the analog input is integrated in a differential integrator, one input of which is the stored error, eliminating the offset and drift components from the integrated output. The time constant of the integrator is not an accuracy-determining factor; indeed, NO COMPONENT OR PARAMETER IS ACCURACY-DETERMINING, EXCEPT THE REFERENCE VOLTAGE STANDARD (and the range-divider resistor ratios, used only on the higher ranges). Finally, in the third phase, the conversion to digital format occurs, returning the integrator to its original zero-state, through the original time constant.

1.2 ISOPOLAR REFERENCING

Isopolar^{R} Referencing for ultimate standardization at low cost. The Isopolar^{R} reference circuit (U.S. patent #3750146) achieves an order-of-magnitude improvement over the conventional zener-diode/inverting-amplifier reference schemes used in most high-performance DMM's. Only ONE zener element is used, regardless of the polarity of the measured voltage. . . a premium-grade, cycle-aged, ultra-stabilized component. It is driven from a highly regulated current source, and housed in a thermally regulated oven. The zener voltage is REACTIVELY coupled to the A/D converter, and isolated from the power-line and digital return grounds, thus preserving the guarded/isolated characteristics of the analog "front-end". Because there is no polarity-inverter error, tracking uncertainty is eliminated. The resultant temperature stability is better than 1PPM/°C, and the ultimate stability fully supports the 6-month rated calibration interval.

1.3 RATIOHMIC RESISTANCE MEASUREMENT

Data Precision pioneered the use of a new approach to resistance measurement (patent applied for), in which the unknown is made part of a RATIO SET, and the excitation of the unknown is a SELF-DETERMINED fraction of the reference standard, simply and passively derived. In this new Ratiohmic approach, reference drift does not affect accuracy, and the instrument combines the inherent accuracy of the ratio set with ultra-high sensitivity.

In addition, the Model 3500 DMM incorporates many high performance capabilities that enhance its usefulness in a wide range of measurement applications. These include:

1.4 INHERENT NOISE REJECTION

In addition to a broadband power-line filter, the Model 3500 design provides exceptionally effective normal-mode rejection inherent in the integrator design. All noise components at frequencies that are integral multiples of 10Hz (i.e., 10Hz, 20Hz, 30Hz, 40Hz. . .etc.) are averaged to zero in the signal integration phase of the tri-phasic conversion. The normal mode rejection is 80dB at 50Hz.

1.5 ULTRAGUARDING

All of the front-end and analog circuits in a Model 3500 are grouped on a compact, electrostatically guarded sector of the main circuit card. This sector contains its own power-supply and regulator supply, which are powered by an isolated, electrostatically guarded winding on the main power transformer, which is TRIPLE-shielded. Input, logic, control, and output interfaces are all effectively isolated. . . many by pulse-transformer coupling.

1.6 DIGITAL INTERFACES

Control and state signals in the Model 3500 are brought to rear-panel connectors, for use in automated control, test, and computing systems applications. Latched BCD data are brought out through standard DTL/TTL interface circuits, and are valid up to the next updating conversion. This permits asynchronous printing, recording, and/or display. These outputs are completely isolated from signal ground, to prevent analog/digital interaction.

RANGE CONTROLS are brought out for remote command, by computer or programmer logic levels, or by remote manual switches. TRIGGER CONTROLS are brought-out, for both remote triggering, and remote trigger inhibiting.

FUNCTIONAL CHARACTERISTICS

1.7 CONVERSION RATE

The longest conversion required is 250 milliseconds. The reading rate when externally triggered may be any rate up to 4 per second. The internally triggered conversion rate is set at 3.3 per second.

1.8 RANGING AND OVERRANGE

The Model 3500 provides both automatic ranging and local or remote manual ranging. Local ranging is by push-button selection. A full 20% overrange, at full accuracy, is provided on all ranges below 1000V.

1.9 INPUT CHARACTERISTICS

In the voltage modes, the input is a true-differential-floating circuit: HIGH/LOW/GUARD. In the ohms mode, a true 4-wire connection is provided: Five standard front-panel binding posts are provided as input connectors for all modes. (Rear-panel input-connector option is described below).

1.10 RATIO MODE (FRONT PANEL)

The 3-wire format of the Model 3500 in ratio mode establishes a correct sense of the ratio and eliminates a ground-loop error path. Ratio polarities are direct-reading. In this mode, the external reference voltage (1 to 11V "source" positive with respect to "sink") is applied to the REFERENCE binding posts, and the input voltage is applied to the HI and LO front panel inputs.

1.11 EXTERNALLY TRIGGERED MODE

In the External Trigger mode, a positive pulse having a duration> 1μsec and <100 millisec, and an amplitude between +2.4V and +5.5V applied to the rear-panel trigger-input terminal, will initiate a single conversion cycle. The resultant reading will be stored and displayed until a new trigger pulse has been received, and a new conversion has been accomplished. . . or until the instrument has been returned to the automatic-triggering mode. Maximum trigger rate, 4 per second for 120% full-scale conversion.

1.12 DISPLAY

1/2" high 7 segment planar premium longlife glow-tube indicators provide numerical display and a polarity symbol, plus overrange indication and automatically positioned decimal point. On manually selected ranges, blinking occurs when the selected range is exceeded. In automatic ranging mode, the meter will automatically select the correct range. Display storage is provided until a new reading (conversion) has been accomplished. . . therefore, the display is steady except for instantaneous transitions to new readings.

STANDARD OPTIONS

OPTION A3: INPUT CABLE. 60" 3-wire cable assembly extends input connections to point of measurement.

OPTION A4: REAR-PANEL INPUT CONNECTOR. Miniature 5-pin connector duplicates front-panel input terminals. Furnished with mating plug.

OPTION A5: RACK-MOUNTING KIT. Specify left or right for DVM. Converts unit to standard 19" x 3 1/2" EIA rack-panel mountings.

OPTION A5/1: DUAL RACK MOUNT. For two Model 3500's or for one Model 3500 and another half-rack instrument.

OPTION A6: MATING CONNECTOR FOR BCD OUTPUT

OPTION A7: CURRENT SHUNT SET. 1mA to 1000mA, AC & DC

Accuracy*: 1mA, 10mA Ranges: ± 0.1% rdg.
100mA, 1000mA Ranges: ± 0.15% rdg.

Temperature Coefficient*: 1mA, 10mA
Ranges: ±0.01%rdg./°C
100mA amd 1000mA
Ranges: ±0.02% rdg./°C

*In addition to the basic specifications of the Model 3500.

Dimensions: 3" high, 5 1/4" wide, and 3" deep.

SCOPE OF INSTRUCTION MANUAL FOR MODEL 3500

This Instruction Manual for Model 3500 DMM contains the general description, principles of operation, operating and maintenance procedures, reference schematics, and parts lists.

The Terms "TRI-PHASIC", "ISOPOLAR", and "RATIOHMIC" are registered trademarks of Data Precision Corporation, and are used to describe proprietary circuits, for which patent applications have been made, or patents have been granted.

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DMM MODEL 3500 SPECIFICATIONS

DC VOLTS

NOMINAL RANGE	OVERRANGE	RESOLUTION	IMPEDANCE	MAXIMUM VOLTAGE
± .100000	± .119999	1μV	>1,000 megohms	± 1000V
± 1.00000	± 1.19999	10μV	>1,000 megohms	± 1000V
± 10.0000	± 11.9999	100μV	>1,000 megohms	± 1000V
± 100.000	± 119.999	1mV	10 megohms	± 1000V
± 1000.00	± 1000.00	10mV	10 megohms	± 1000V

ACCURACY

4 upper ranges, including overrange	
24 hours, 23°C ± 1°C	± 0.004% rdg. ±0.001% f.s. ± 1 l.s.d.
6 months, 23°C ± 5°C	± 0.007% rdg. ±0.001% f.s. ± 1 l.s.d.
lowest range:	
24 hours, 23°C ± 1°C	± 0.005% rdg. ± 0.003% f.s. ± 1 l.s.d.
6 months, 23°C ± 5°C	± 0.008% rdg. ± 0.003% f.s. ± 1 l.s.d.

VOLTAGE COEFFICIENT **(Generally applicable only on highest range)**

Add ± 0.00001% rdg./Volt

TEMPERATURE COEFFICIENT (0°C to 50°C)

4 upper ranges:	(± 0.001% rdg. ± 0.0002% f.s.)/°C
lowest range:	(± 0.001% rdg. ± 0.0005% f.s.)/°C

COMMON-MODE REJECTION RATIOS **(minimum):**

at DC, **160dB with 1000 Ohm source-impedance unbalance**

at 60Hz, **120dB with 1000 Ohm source-impedance unbalance**

COMMON-MODE VOLTAGE: **400V DC (or Peak AC) maximum.**

NORMAL-MODE REJECTION RATIO: **80dB at 50Hz and every 10Hz increment thereafter**

AC VOLTS

NOMINAL RANGE	OVERRANGE	RESOLUTION
.100000	.119999	1μV
1.00000	1.19999	10μV
10.0000	11.9999	100μV
100.000	119.999	1mV
1000.00*	1000.00*	10mV

***See maximum voltage limitation, below**

INPUT IMPEDANCE (all ranges): **1 megohm in parallel with 100pF or less.**

SENSING & CALIBRATION: **True-Average sensing calibrated in RMS of sinewave.**

ACCURACY (6 months, 23°C ± 5°C):

	FOUR UPPER RANGES	.1V RANGE
at 30 Hz	± 1% rdg. ± 0.02% f.s.	± 1% rdg. ± 0.1% f.s.
50Hz - 1kHz	± 0.05% rdg. ± 0.02% f.s.	± 0.05% rdg. ± 0.1% f.s.
10kHz	± 0.2% rdg. ± 0.02% f.s.	± 0.2% rdg. ± 0.1% f.s.
100kHz	± 1% rdg. ± 0.05% f.s.	± 1% rdg. ± 0.5% f.s.

TEMPERATURE COEFFICIENT (0°C to 50°C, all ranges):

Four Upper Ranges:

30Hz - 1kHz	(± 0.005% rdg. ± 0.002% f.s.)/°C
1kHz - 10kHz	(± (0.005 x freq. in kHz) % rdg. ± 0.002% f.s.)/°C
10kHz - 100kHz	(± 0.05% rdg. ± 0.002% f.s.)/°C

0.1V Range:

30Hz - 1kHz	(± 0.005% rdg. ± 0.02% f.s.)/°C
1kHz - 10kHz	(± (0.005 x freq. in kHz) % rdg. ± 0.02% f.s.)/°C
10kHz - 100kHz	(± 0.05% rdg. ± 0.02% f.s.)/°C

MAXIMUM INPUT VOLTAGE (sinewave RMS):

30Hz to 10kHz: 700V

above 10kHz: Decreases linearly to 100V at 100kHz

SETTLING TIME (to settle within ± 0.05% of final reading for a full-scale step input): 2.5 seconds

---

OHMS

NOMINAL RANGE	OVERRANGE	RESOLUTION	MAX. TEST CURRENT
.100000kΩ	.119999kΩ	1 milliohm	1mA
1.00000kΩ	1.19999kΩ	10 milliohms	1mA
10.0000kΩ	11.9999kΩ	100 milliohms	100μA
100.000kΩ	119.999kΩ	1 Ohm	10μA
1000.00kΩ	1199.99kΩ	10 Ohms	1μA
10000.0kΩ	11999.9kΩ	100 Ohms	0.1μA

CONFIGURATION: True four-wire.

MAXIMUM OPEN CIRCUIT VOLTAGE: 6.2 Volts.

ACCURACY (6 months, 23°C ± 5°C):

.1kΩ range	± 0.008% rdg. ± 0.003% f.s. ± 1 l.s.d.
1kΩ/10kΩ/100kΩ ranges	± 0.007% rdg. ± 0.001% f.s. ± 1 l.s.d.
1000kΩ range	± 0.02% rdg. ± 0.002% f.s. ± 1 l.s.d.
10,000kΩ range	± 0.2% rdg. ± 0.01% f.s. ± 1 l.s.d.

TEMPERATURE COEFFICIENT (0°C to 50°C):

.1kΩ range	(± 0.001% rdg. ± 0.001% f.s.)/°C
1kΩ/10kΩ/100kΩ ranges	(± 0.001% rdg. ± 0.0004% f.s.)/°C
1 megΩ range	(± 0.005% rdg. ± 0.0004% f.s.)/°C
10 megΩ range	(± 0.02% rdg. ± 0.005% f.s.)/°C

SETTLING TIME (to settle to within ± 0.01% of final reading): in seconds for any resistance = 0.1 +0.3 x resistance in megohms.

Max. Input Voltage: ± 150V peak, or 115V AC (RMS)

DC RATIO

SELECTED RANGE	NOMINAL RANGE	OVERRANGE	ACTUAL DISPLAY*
.1	± .0100000:1	±.0119999:1	± .119999
1	± .100000:1	± .119999:1	± 1.19999
10	± 1.00000:1	± 1.19999:1	± 11.9999
100	± 10.0000:1	± 11.9999:1	± 119.999
1000	± 100.000:1	± 119.999:1	± 1199.99

*Displayed Ratio is 10 time true ratio

ACCURACY:

Upper Ranges, 24 hours, 23° ± 1°C:

$$(\pm 0.004\%\ \text{rdg.} \pm 0.001\%\ \text{f.s.} \pm 1\ \text{l.s.d.}) \times \frac{10}{\text{Actual Ref. Voltage}}$$

Lowest Range, 24 hours, 23° ± 1°C:

$$(\pm 0.005\%\ \text{rdg.} \pm 0.004\%\ \text{f.s.} \pm 1\ \text{l.s.d.}) \times \frac{10}{\text{Actual Ref. Voltage}}$$

Upper Ranges, 6 months, 23°C ± 5°C:

$$(\pm 0.008\%\ \text{rdg.} \pm 0.001\%\ \text{f.s.} \pm 1\ \text{l.s.d.}) \times \frac{10}{\text{Actual Ref. Voltage}}$$

Lowest Range, 6 months, 23°C ± 5°C:

$$(\pm 0.008\%\ \text{rdg.} \pm 0.003\%\ \text{f.s.} \pm 1\ \text{l.s.d.}) \times \frac{10}{\text{Actual Ref. Voltage}}$$

TEMPERATURE COEFFICENT ($0^{o}C$ to $50^{o}C$, all ranges):

Upper Ranges: $(\pm 0.001\%\ \text{rdg.} \pm 0.0002\%\ \text{f.s.}) \times \frac{10}{\text{Actual Ref. Voltage}} /^{o}C$

Lowest Range: $(\pm 0.001\%\ \text{rdg.} \pm 0.001\%\ \text{f.s.}) \times \frac{10}{\text{Actual Ref. Voltage}} /^{o}C$

VOLTAGE COEFFICIENT OF RATIO: ± 0.00001% rdg/Volt

VOLTAGE RANGE:		
	Input Signal:	0 to ± 1000V
	Reference Signal:	+1V to +11V

REFERENCE INPUT IMPEDANCE: 100k

COMMON-MODE REJECTION RATIO: Same as DC Volts

NORMAL MODE REJECTION RATIO: Same as DC Volts

INTERFACE AND APPLICATION SPECIFICATIONS

SIGNAL INTERFACES

DATA OUTPUTS (DTL/TTL compatible) BCD 1-2-4-8 coded, positive true.

Logic ONE: > +2.4V
Logic ZERO< +0.4V sink for 4mA
Polarity output, One = Positive polarity

STATE OUTPUTS (DTL/TTL compatible)

Range in use = ZERO:< +0.4 sink for 4mA
Inactive ranges = ONE: >+2.4V
End of Conversion is transition from ZERO to ONE.

CONTROL INPUTS.

RANGE: Each range is selected by the grounding of the appropriate line, through switch contacts or grounded transistor.

EXTERNAL TRIGGER:

Positive pulse 2.4 volts with a pulse width of >1μsec., and <100 msec will initiate a read command. The command will cause the instrument to perform one measurement. The reading will remain in the memory until a new external trigger pulse is initiated.

TRIGGER INHIBIT INPUT (Applying logic "0" inhibits conversion in all trigger modes):

Logic "1" >+2.4V

Logic "0" < +0.4V sink for 4mA

INPUT POWER: 105V-125V AC (or 210-250V AC) 47-63 Hz, less than 12 Watts. Line-voltage range is selected by rear panel switch.

ENVIRONMENT

TEMPERATURE RANGES: Operating, 0°C to +50°C
Storage, -25°C to +80°C

HUMIDITY: 95% RH max, 0°C to 40°C
80% RH max, +40°C to +50°C

OVERALL DIMENSIONS: 3 1/2" high, 8 1/2" wide, and 12" deep, including panel controls and connectors.

WEIGHT: 8 pounds net, 14 pounds packed for domestic shipment.

STAND: Adjustable, removable, tilt-up stand provided for best viewing in bench use.

Chapter 2

OPERATION

2.1 UNPACKING

The Model 3500 digital multimeter is shipped in a protective packing case containing the following items:

One digital multimeter, with line cord (3-wire) attached
One instruction manual,
One certificate of traceability to NBS Standards,
One warranty card, and
One copy of the test and inspection data for the instrument.

If the carton showed signs of rough handling or damage, inspect the multimeter carefully and report the damage to the shipping company immediately. Fill out the warranty card as directed and return it to the factory.

2.2 OPERATING CONTROLS AND INDICATORS

The front panel controls and indicators are identified in Figure 2-1, and their functions are described in Table 2-1. The rear panel controls are identified in Figure 2-2, and are described in Table 2-2.

2.3 POWER CONNECTIONS

Model 3500 DMM is shipped with the power switch preset for the AC voltage source anticipated in the user area and the setting is recorded on the Test Data Sheet forwarded with the instrument. (In the United States this is 115V.) The AC source selection switch, S201, is located on the rear panel of the DMM, and its setting may be changed, if necessary. Use a small-blade screw driver to set S201 to the proper value as stamped on switch.

2.4 GUARD CONNECTIONS

Instrument construction provides a GUARD circuit connected to the internal shield surrounding the analog and A/D sections of the instrument and isolated from any analog input or external ground. Prior to any measurement, a proper GUARD connection must be made in order to bring the internal shield as close as possible to the voltage potential of the low side of the input circuit. The low side of the input is separated from internal grounds and is brought out as a front panel connection where it may be connected as required.

The GUARD connection should be made to minimize the common mode currents through the voltage measuring circuit, and it should be connected to the low side as close to the voltage source as possible. If it is not feasible to connect at the source, make the connection between GUARD and the low side of the input at the DMM front panel.

2.5 RANGING

a. Manual Ranging

The DMM is a direct reading instrument in any voltage or resistance range setting, and displays ten times the actual when making Ratio measurement. When any one of the fixed ranges is chosen, the display will automatically indicate correct polarity of high input terminal referred to low (in DC), and will read the input voltage to 5 1/2 significant figures (up to 119999). An out-of-range input signal will result in two effects simultaneously - -

1. A 120000 reading on the display (and decimal point).
2. A blinking "1" in the most significant digit.

When the DMM is switched to the correct range, the reading will be steady at less than 120000.

Zero's in the most significant digits indicate that the full scale range may be decreased. Full resolution capability of the instrument is being used when the reading is between 010000 and 119999, 10% to 120% of full scale, with proper decimal point location.

b. Auto Ranging

When AUTO is selected at the front panel, the meter automatically settles at that range where the reading is

Table 2-1

FRONT PANEL CONTROLS AND INDICATORS

NOTE

Complete operating instructions follow the description of controls and indicators.

Fig. Ref.	Control/ Indicator	Description	Function
1.	POWER	Push-push switch	Applies power to the DMM from connected source.
2.	DC	Push switch	Selects DC voltage measurement mode of DMM operation. Is interlocked with other mode selectors; is pushed out when other mode is selected.
3.	AC	Push switch	Selects AC voltage measurement mode of DMM action. Is interlocked with other modes so that it is pushed out upon selection of another mode.
4.	kΩ	Push switch	Selects resistance measurement mode of DMM operation. Is interlocked with other modes so that it is pushed out upon selection of another mode.
5.	Vx	Two 5-way binding posts	Connection for input voltage, AC or DC, or resistance.
6.	Rx	Two 5-way binding posts	Current source and sink terminals for resistance connection. Connection for voltage ratio reference Input.
7.	GUARD	One 5-way binding post	External connection to guard shield.
8.	DISPLAY	7-segment planar indicators	Displays digital readout for a maximum of 120000. Decimal point is selected automatically and indicates value of a direct reading. Sign is displayed automatically when in DC measurement mode.
9.	RANGE .1 1 10 100 1K 10K	Push switch for manual range selection	Selects value of full scale range to be used by DMM in measuring input. Is interlocked so that only one may be in at a time. 10K for use with KΩ function only.
10.	AUTO	Push switch for automatic range selection	Initiates DMM operation to locate range for which the input signal will be measured between 10% and 120% of full scale.
11.	RATIO	Push switch	Selects RATIO measurement mode of DMM operation. It is not interlocked with other modes and must be depressed to release. Used in conjunction with DC button for DC/DC RATIO or AC button for AC/DC RATIO.

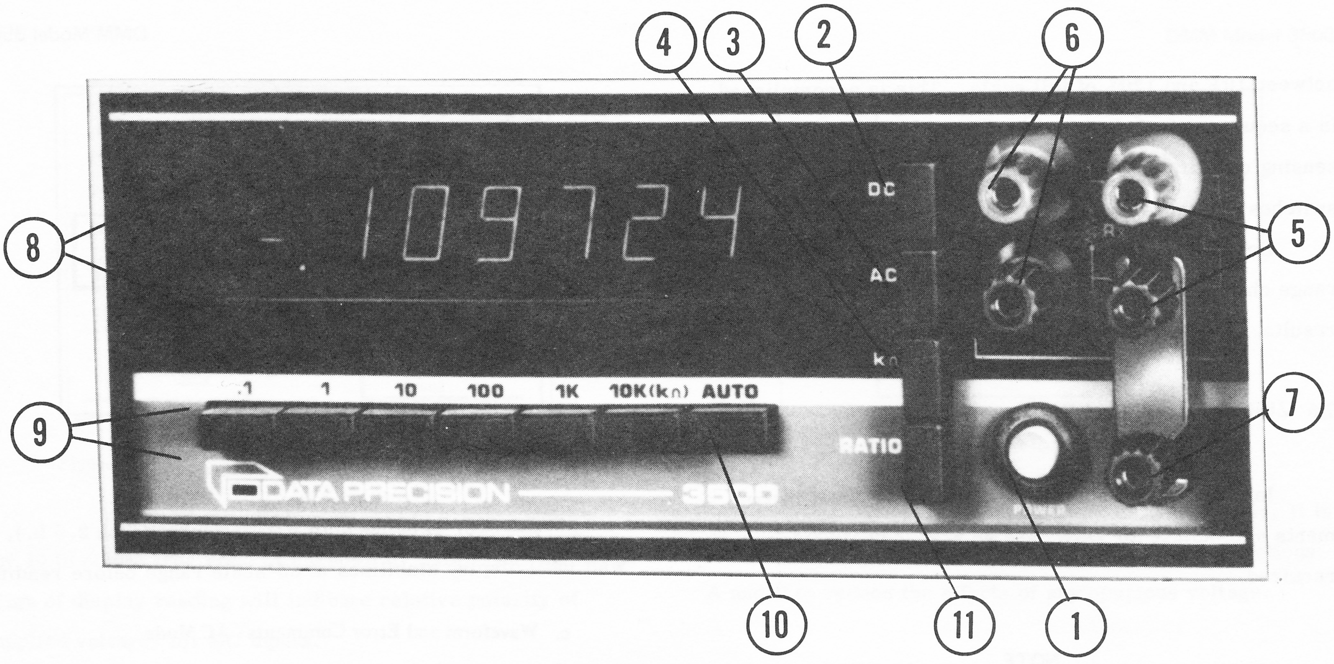
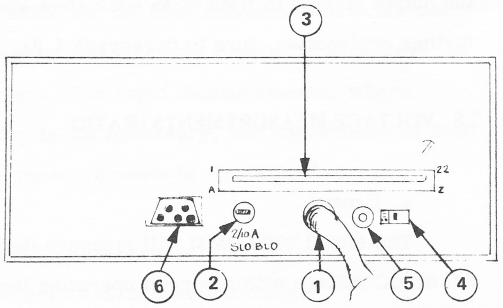

4
3
2
6
8
5
9
7
10
11
1
-109724
DC
AC
kΩ
.1
1
10
100
1K
10K(kΩ)
AUTO
RATIO
DATA PRECISION
3500

Figure 2-1 Model 3500 Front Panel Controls and Indicators


3
1
A
22
Z
2/10 A
SLO BLO
6
2
1
5
4

ITEM 5 IS A REAR PANEL CHASSIS GROUND BINDING POST

ITEM 6 IS A REAR PANEL CONNECTOR FOR SIGNAL INPUTS: SEE LIST OF OPTIONS.

Figure 2-2 Model 3500 Rear Panel Controls and Indicators

Table 2-2

REAR PANEL CONTROLS AND INDICATORS

Fig. Ref.	Control/ Indicator	Description	Function
1.	POWER CORD	3-conductor cord	Connects source power to instrument.
2.	FUSE	Receptacle and holder	For a 2/10 amp slow-blow line fuse.
3.	REMOTE	PC Connector	Provides digital output of measured value, indicates selected range of operation, and provides input for remote control of range and remote triggering of DMM operations. (See Table 2-3).
4.	LINE VOLTAGE SWITCH	115/230V switch	Connects proper transformer voltage taps so that Series 2000 will work in user area.

between 10% and 120% of full scale. This is accomplished in a sequence of conversions, after each of which the range sensing circuit performs a decision-function analysis and switches the range scale until the correct one is chosen.

Decimal point indications on the display follows each range change to update the display for direct reading results.

2.6 ZEROING

In all modes of operation, Model 3500 DMM instruments self-adjust for zero, and no zero-adjustment is required.

NOTE

If no input is connected to the instrument and a sensitive range is selected, spurious readings may appear because of the high impedance input. These are of no consequence and do not indicate any incorrect performance when the instrument is properly connected for use.

2.7 VOLTAGE MEASUREMENTS

a. General

The same procedure is used in AC voltage and DC voltage measurements. Precautions to avoid pickup and stray signals should be strictly observed because high frequency spurious inputs may be mistaken for acceptable signals in the AC measuring mode. Refer to paragraph 2.4 for information on GUARD connection. If possible, enclose both input leads in a shield and connect the shield to GUARD at the instrument end, and to the low side of signal at the source end.

b. Procedure

(See paragraph 2.8 for Ratio.)

1. Select appropriate voltage measurement mode, AC or DC.

2. Connect input circuit to Vx (Figure 2-3). (Link A and B may be left in place).

3. Make appropriate GUARD connections.

4. a) If using Manual Ranging (paragraph 2.5 a.), select most sensitive range that does not cause DMM to indicate an overrange condition. This will utilize full 5 digits of DMM resolution capability.

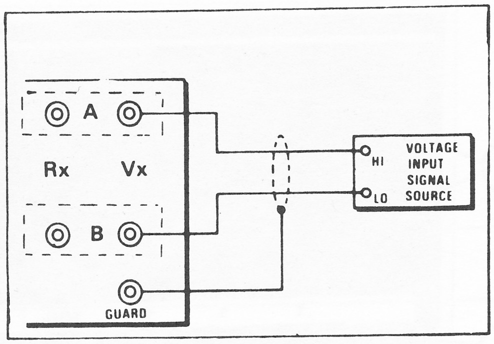


Figure 2-3. Voltage Measurement Connections

b) If using Auto Ranging (paragraph 2.5 b.), wait until display stabilizes at on-scale range before reading.

c. Waveform and Error Comments - AC Mode

In measuring input AC voltages, the DMM circuitry blocks any incoming DC, and the instrument operates within specification accuracy for any superimposed DC voltage up to 500 volts. The DMM measures the average value of one-half cycle of the resulting AC waveform, and calibrates the output display in RMS of an equivalent sine wave. (For further explanation, turn to paragraph 4.3)

2.8 VOLTAGE MEASUREMENTS (RATIO)

a. General

The Model 3500 DMM will measure the ratio of any AC or DC voltage within normal operating limits referenced to an external DC reference voltage between +1 volt and +11 volts. The displayed ratio value will be 10 times the true ratio.

b. Procedure

1. Press RATIO push button at Front Panel (Figure 2-1).

2. Select appropriate AC or DC mode.

3. Select appropriate manual range or auto range.

4. Install links as shown in Figure 2-4. (Link B may be omitted.)

5. Connect voltage input signal to the front panel Vx connectors as in Figure 2-4.

6. Connect the reference voltage input signal to the front panel Rx connectors as shown in Figure 2-4.

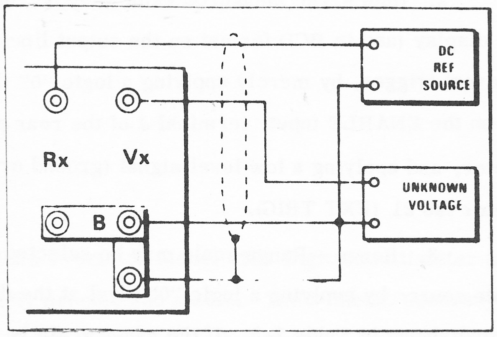


Figure 2-4. DMM Connections for RATIO Measurement

7. Read output after display is stable. Divide by 10 to obtain true ratio of unknown to known reference. Sign of display reading will indicate relative polarity of applied voltages for DC inputs.

2.9 RESISTANCE MEASUREMENT

a. General

The Model 3500 DMM measures any resistor between .119999 kΩ full scale and 11.9999 megohms full scale and offers full four-wire measurement capability to achieve the specified accuracy. For rapid measurements, where extreme accuracy is not necessary, the convenience of two-wire resistance measurements is also afforded.

b. Four-Wire Measurements

1. Select kΩ measurement mode.

2. Connect the Vx terminals to inner connection points, A, of the unknown resistor as shown in Figure 2-5.

3. Connect the current source and sink to the outer connection points, B, of the unknown resistor as shown in Figure 2-5.

4. Connect guard to the low side (current sink) of the circuit as shown in Figure 2-5.

5. Select appropriate autorange of manual range switch for expected resistance. Note that highest range of 10K kilohms = 10 megohms is available in resistance measurement mode.

6. Observe display. As soon as decimal point location is stable, a correct reading may be made. An over range condition will result in a blinking indication as in voltage measurements (see paragraph 2.5a).

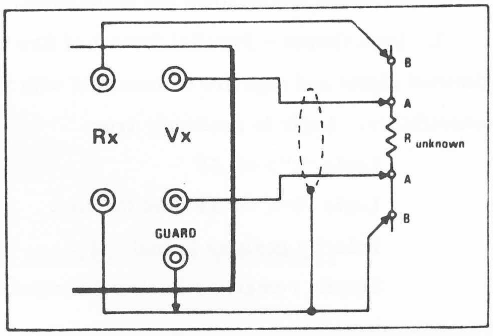


Figure 2-5. Four-Wire Resistance Measurement

7. When measuring high resistance values, it is desirable to shield the resistor through to the connections A and B to reduce the effects of any spurious voltage.

c. Two-Wire Measurements

When making two-wire resistance measurements, connect the unknown resistance and the current source and sink to the connection points as shown in Figure 2-6. Perform the measurement as in steps 4. through 7. in paragraph 2.9a above. (Links must be connected as shown.)

2.10 REMOTE OPERATION

a. Set-Up

To obtain remote control and to transmit data from Model 3500 DMM - -

1. Prepare a cable with 44-pin connector VIKING 2VK22D/1-3 or equivalent, and cabled as shown in Table 2-3.

2. Remove protective covering from the PC Board connector at Rear Panel and connect cabled connector.

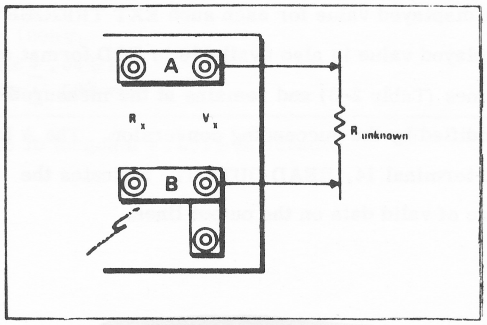


Figure 2-6 Two-Wire Resistance Measurement

b. **Output Signals Specifications and Applications**

1. Data Output - Parallel format of five binary-coded decimal digits and sign are transmitted with DTL/ T^2L compatibility. Logic is positively true:

Logic "1"> +2.4V
Logic "0"< +0.4V sink for 4mA
Polarity positive is logic "1".
Signals remain as latched on output lines between conversions.

2. Range scale in use is indicated by logic "0". Inactive ranges are logic "1"'s.

(Decimal point is determined and indicated by range in use.)

3. Completion of the conversion (EOC) is indicated by an internal control signal, and is followed immediately by the update of the Display. The availability of updated data is indicated by the READOUT signal on connector tab 14. Valid data outputs are available after the rising edge of the READOUT waveform.

4. Overload - A zero logic level on this line indicates the input of a signal more than 120% of the selected full scale range, necessitating a range change. This output thus serves to indicate existence of incorrect data on the output lines and may be used to inhibit input of incorrect data to receiving printers, computers, etc. It also transmits a short negative pulse at EOC.

c. **Remote Control**

1. Conversion - In order to exercise a remote control of the conversion, two signals are required: ENABLE, a low level on terminal J to inhibit the internal triggering, and EXT. TRIGGER, a 2.4V positive pulse between 1μsec and 100 milliseconds wide applied to terminal 21. The Model 3500 DMM will make one conversion and hold the displayed value for each such EXT TRIGGER pulse. The displayed value is also available in BCD format on the output lines (Table 2-3) and remains at the measured value until modified by the succeeding conversion. The A high level on terminal 14, READ OUTPUT, indicates the existence of valid data on the output lines.

2. Hold - The measured value may be retained on the display (and in BCD format on the output lines) while on internal trigger, by merely applying a logic "0" (low level) on the ENABLE input, terminal J of the rear panel connector, and applying a low level signal (ground or logic) to connector tab 21 (EXT TRIG).

3. Range - Range scale may be selected from a remote source by applying a logic "0" level at the designated terminal shown in Table 2-3. If the range scale is not externally selected, the appearance of a low level on these terminals indicates the range scale for the measurement value in BCD format on data output lines. Make sure all Range buttons are out.

Table 2-3

REMOTE CONTROL/OUTPUT CABLE			
A	Ground	1	Ground
B	$\overline{10^1}$	2	8
C	8,000	3	4
D	4,000	4	2
E	2,000	5	1
F	1,000	6	$\overline{10^4}$
H	$\overline{10^0}$	7	80
J	Enable	8	40
K	NC	9	20
L	NC	10	10
M	NC	11	$\overline{10^3}$
N	800	12	NC
P	400	13	NC
R	200	14	Read Output
S	100	15	80,000
T	$\overline{10^2}$	16	40,000
U	NC	17	20,000
V	NC	18	10,000
W	NC	19	100,000
X	$\overline{10^{-1}}$	20	+
Y	$\overline{\text{Overload}}$	21	Ext. Trig.
Z	Ground	22	Ground

Chapter 3

CALIBRATION

Data Precision Model 3500 Digital Multimeter is extremely precise and stable. The 6-month accuracy should last for longer than the specified period. It is advisable to check the instrument periodically. When doing so, follow all procedures carefully and observe all precautions.

3.1 CALIBRATION VERIFICATION

Data Precision Corporation recommends establishing and maintaining a performance history log. Transfer the certified factory performance test data as the initial entry. In order to have a locally available test performance for comparison, it is suggested that the instrument be tested against an available standard as soon as it is unpacked and the test results be recorded at that time. The instrument should be checked thereafter at least every six months.

3.2 PRELIMINARY SET UP CONDITIONS

a. Establish a solid ground connection from the case to the power source ground. If the third wire of the three-wire power cord does not carry through to main power ground, ground the meter case with a clip lead attachment.

b. Accuracy of standards used to calibrate the multimeter should be verified before recalibrating the instrument. Errors of standards should be no worse than 20% of the tolerances specified for the multimeter.

3.3 CALIBRATING EQUIPMENT

The following equipment is recommended for use when called out in the calibration procedure. Substitute units may be employed provided they meet the accuracy characteristics specified below.

Feature Under Test	Standard Type Model No.	Accuracy Requirements
DC Volts Measurement	COHU/Model 355	10V range ± .001% rdg +2µV 100V range ± .001% rdg +20µV 1000V range ± .001% rdg +40µV 1000V range ± .001% rdg +40µV
AC volts	HP/Model 745A and 746A	1mV to 100V: 50Hz-20kHz ± .02% rdg ± .002% range ± 10µV 20Hz-100kHz ± .05% rdg ± .005% range ± 50µV 100V to 1000V: 50Hz-20kHz ± .04% rdg 20Hz-50kHz ± .08% rdg
Resistance	JULIE NB-102-100Ω (.001%) JULIE/DMR-105A (.001%) JULIE/NB-106-1M (.0015%) JULIE/NB-107-10M (.003%)	1 kilohm to 10 megohm ± .001% in decades

Table of Recommended Calibrating Equipment

3.4 ACCESS TO CALIBRATION ADJUSTMENTS

All calibration adjustments are accessible after the top cover has been removed (see Figure 3-1). The actual calibration potentiometers are mounted on the circuit board, but may be reached through an opening provided in the guard shield. A summary table of the Calibration Procedure is located on the inside top cover of the instrument.

CAUTION

Do not remove the Guard during Calibration Process.

3.5 CALIBRATING SEQUENCE

Perform the calibration in the following sequence of measurement modes:

1. DC Voltage Measurement Mode
2. Resistance Measurement Mode
3. AC Voltage Measurement Mode
4. Ratio Measurement Mode.

3.6 DC VOLTAGE MEASUREMENT MODE

Depress "ON" switch; wait one hour for calibration.

a. Zero Adjust: R300, R45, R46

1. Select DC Volts Mode
2. Select .1V Full Scale
3. Connect shorting bar across input, Vx
4. Adjust R300 for ± 0.00000 display value
5. Set range to 10V Full Scale
6. Connect 10-megohm (approx) resistance across input Vx
7. Adjust R45 for ± 0.00000 display value
8. Connect shorting bar across input Vx
9. Adjust R46 for ± 0.00000 display value
10. Repeat steps 6 through 9 as necessary.

b. Balance Adjust: R83

1. Set Range to 1V Full Scale
2. Apply 1V (approx) to input Vx
3. Read display, Record.

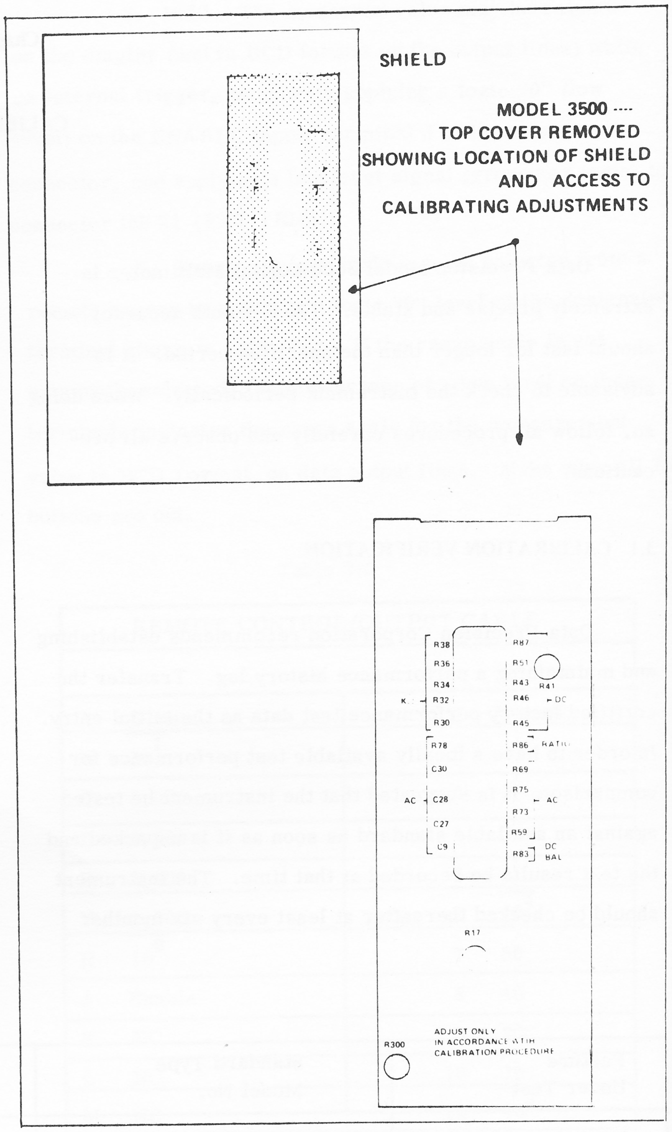

SHIELD
MODEL 3500 ----
TOP COVER REMOVED
SHOWING LOCATION OF SHIELD
AND ACCESS TO
CALIBRATING ADJUSTMENTS
R38
R36
R34
K
R32
R30
R78
C30
AC
C28
C27
C9
R87
R51
R41
R43
R46
DC
R45
R86
RATIO
R69
R75
AC
R73
R59
R83
DC
BAL
R17
R300
ADJUST ONLY
IN ACCORDANCE WITH
CALIBRATION PROCEDURE

Figure 3-1 Location and Identification of Calibrating Adjustments

4. Reverse input polarity. Record
5. Adjust R83 until values of step step 3. and 4. are exactly same on display
6. Repeat steps 3 through 5 as necessary.

c. Reading Adjustments

For each full scale range, apply positive full scale voltage and adjust the appropriate potentiometer for full scale value on the display.

Set F.S. Range to	Adjust	For reading of
1) 1-Volt Range	R87	+1.00000
2) .1-Volt Range	R17	+.100000
3) 10-Volt Range	R51	+10.0000
4) 100-Volt Range	R43	+100.000

3.7 RESISTANCE MEASUREMENT MODE

Turn unit "ON". Depress KΩ mode switch.

NOTE

Calibration is accomplished using the 4-wire resistance set-up (Figure 2-5). Adjust until display reads known value of resistor.

Set F.S. Range to	Range Switch	Connect R Value of ohms	Adjust	For Reading of
1 k ohm	1	1.00000 k	R30	1.00000
10 k ohm	10	10.0000 k	R32	10.0000
100 k ohm	100	100.000 k	R34	100.000
1,000 k ohm	1k	1.00000 M	R38	1000.00*
10k k ohm	10k	10.000 M	R36	10000.0*

*Noise may obliterate last decade.

3.8 AC VOLTAGE MEASUREMENT MODE

NOTE

Connect LO voltage input to Guard. Check signal source to assure that it is free of harmonics.

a. Select AC-Volt Mode

b. Zero Adjust: R59

1. Select 100V full scale range
2. Connect shorting bar across Vx
3. Adjust R59 for display reading of 000.000

c. Low Frequency Full Scale Adjustments

At a frequency of appriximately 100 Hz, apply the designated voltage to terminals Vx, and adjust the appropriate calibrating potentiometer for the indicated display reading.

Set F.S. Range to	Apply VRMS to Vx	Adjust	For Reading of
1	1.00000	R69	1.0000
10	10.0000	R73	10.000
100	100.000	R75	100.00
1K	500.00	R78	0500.0

d. High Requency Full Scale Adjustments

Change frequency of signal generator to approximately 50 kHz, apply the designated voltage to terminals Vx, and adjust the designated calibrating adjustment for the designated display reading. Use insulated H. F. type tweeking tool.

Set F.S. Range to	Apply VRMS to Vx	Adjust	For Reading of
1K	0200.00	C9	0200.0
100	100.000	C30	100.00
10	10.0000	C28	10.000
1	1.00000	C27	1.0000

3.9 RATIO DC VOLTAGE MEASUREMENT MODE

a. Select DC voltage and push the RATIO button at the front panel.

b. Apply full scale (+10V DC) simultaneously to the Vx input and to the Rx input in parallel to front panel.

c. Adjust calibrating potentiometer R86 for a reading of +10.0000.

3.10 POST-CALIBRATION

As calibration is completed, enter data below and initial. Turn off power. Reassemble unit by replacing cover.

DATE	CALIBRATION RECORD

Chapter 4

PRINCIPLES OF OPERATION

4.1 GENERAL

The principles of operation of Model 3500 DMM are presented in two main subdivisions. Initially, in paragraph 4.1 through 4.6, the functional performance of each of the major subsystems is presented in brief. This is intended to provide an understanding of the general function of the unit: of how the different types of input signals are processed through to the display in the various modes of operation. The remainder of Section 4 contains detailed circuit explanations. Such material is useful for further study and understanding of the instrument operation and for detailed corrective maintenance, but may be omitted until needed without detracting from the effective use of the Model 3500 DMM.

4.2 SYSTEM BLOCK DIAGRAM

In its simplest form, the DMM is represented by the Block Diagram of Figure 4-1. The system consists of an input Signal Conditioning block, followed by the TRI-PHASIC™ Analog to Digital (A/D) Converter block, whose decoded outputs are driving signals for the Timing and Display block. The Timing & Control block and two Power Supply blocks complete the unit.

The major blocks in Figure 4-1 physically comprise the following:

Analog Block Diagram
(Figure 4-2)
Digital Block Diagram
(Figure 4-3),

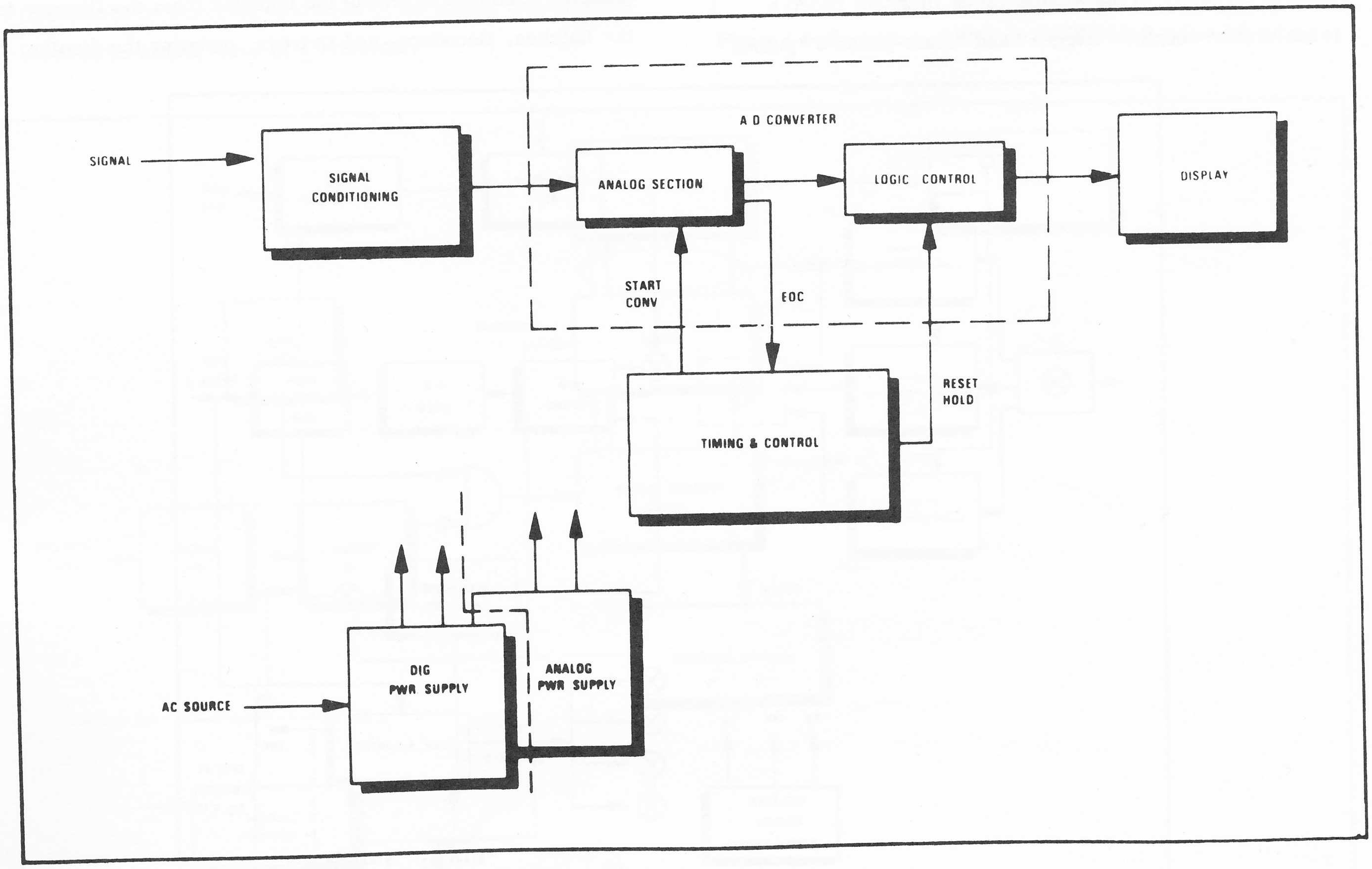

SIGNAL
SIGNAL CONDITIONING
A D CONVERTER
ANALOG SECTION
LOGIC CONTROL
DISPLAY
START CONV
EOC
RESET HOLD
TIMING & CONTROL
DIG PWR SUPPLY
ANALOG PWR SUPPLY
AC SOURCE

Figure 4-1. Simplified Block Diagram

The analog portion of the TRI-PHASIC A/D converter accomplishes the conversion in the three phases of (1) self zeroing, (2) unknown integration, and (3) reference integration, the latter two compensated by the stored value of compensating offset.

In the Analog Block Diagram (Figure 4-2), one of the three signal conditioning blocks (for Resistance, DC Volts, and AC Volts measurements) is connected via a switching network as the input to the A/D preamplifier. The preamplifier output is intergrated and then processed by the high gain amplifier. The high gain amplifier outputs: (1) drive the sign indicator at the end of phase 2 to obtain the switching control signals that select the appropriate polarity of the ISOPOLAR^{TM} reference voltage to be applied (via the switching network) to the A/D preamplifier in phase 3 and at the same time drive the Display to indicate sign, and (2) indicate end of phase 3. The high gain amplifier in phase 1 also drives the self zeroing circuitry to develop the offset signal to be applied during the phases 2 and 3 as an input to the A/D preamplifier. Logic and Control circuitry in the Analog Block Diagram receive transformer-coupled "trigger" and "start-phase 3" pulses from the digital blocks to initiate phase 2 and phase 3 converter action, respectively, in each conversion cycle and develop end of conversion pulses to be transmitted via transformer coupling to the digital blocks to end phase 3. An isolated and triple-shielded Analog Power Supply furnishing ± 15V and -5V completes the DMM Analog Block section.

In the Digital Block Diagram (Figure 4-3), the Trigger block generates a control pulse (from its own internal timing circuitry or from external command) as the "start convert" command to the Enable FF. If not blocked by the External Enable signal, the Enable FF gate permits the Crystal Clock pulses to drive the Decade Counter Chain block to start phase 2 operation. At 100,000 counts (end of phase 2) a carry pulse (10^5 CARRY) is transmitted to the Analog Block to start phase 3, while the decade chain continues its counting. When an EOC pulse is received from the Analog Block, the digital control block applies a stop command to the Enable FF stopping the count. At the same time, the Control block generates a transfer command to enable the transfer from the Counter to the Latches, Decoders, and Drivers, updating the display.

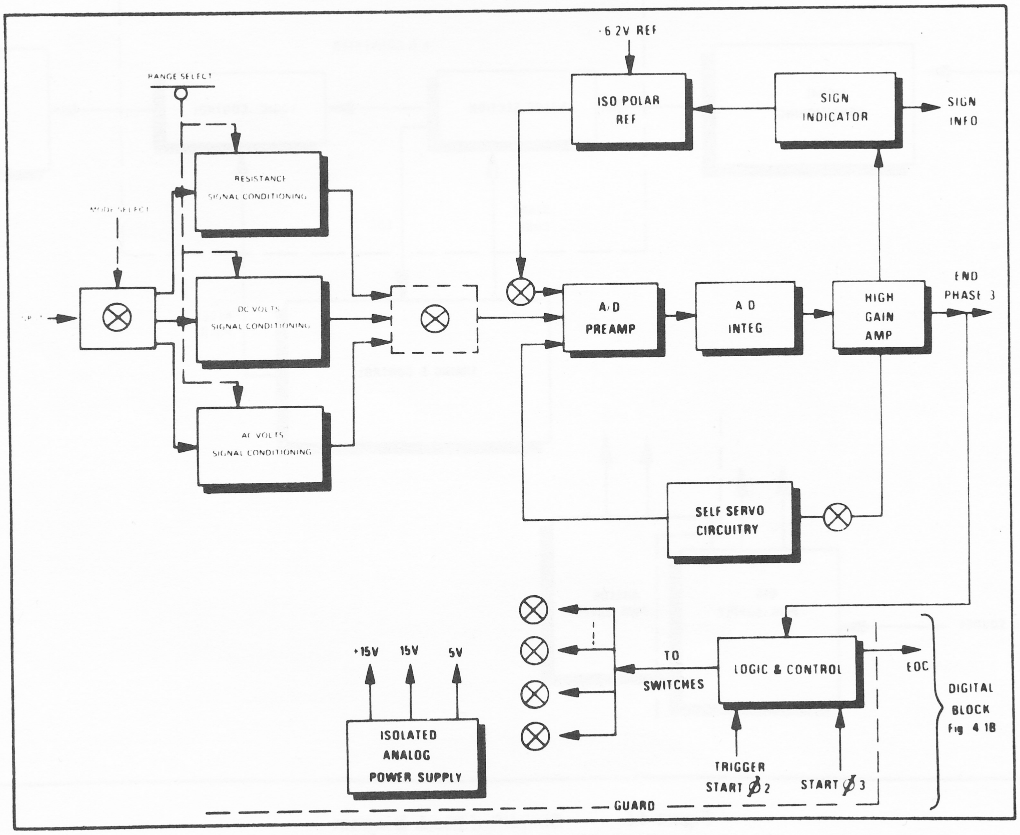

6.2V REF
RANGE SELECT
ISO POLAR REF
SIGN INDICATOR
SIGN INFO
MODE SELECT
RESISTANCE SIGNAL CONDITIONING
DC VOLTS SIGNAL CONDITIONING
AC VOLTS SIGNAL CONDITIONING
A/D PREAMP
A D INTEG
HIGH GAIN AMP
END PHASE 3
SELF SERVO CIRCUITRY
+15V
15V
5V
ISOLATED ANALOG POWER SUPPLY
TO SWITCHES
LOGIC & CONTROL
EOC
DIGITAL BLOCK Fig 4 18
TRIGGER START ∅2
START ∅3
GUARD

Figure 4-2 Model 3500 Analog Block Diagram

The updated count (at end of conversion) is held in the Latch and the Display until the next update and is also available as BCD output from the Latch block for remote data output applications.

The Range Select block is driven by one of three sources: manual range selection, remote range selection, or (when in auto range) a command developed when the range of a particular conversion results in a phase 3 count of less than 10,000 or more than 119,999.

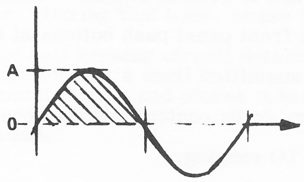
Paragraphs that follow now trace the signal through the functional blocks of Figures 4-1, 4-2, and 4-3.

4.3 SIGNAL CONDITIONING BLOCK
(Figure 4-2)

An input signal to be measured is introduced into the Signal Conditioning block where it is attenuated according to the range scale chosen, so that a normalized full scale value of ± 1.0 volts DC is delivered to the A/D Converter lock. Overrange capability of 120% of full scale is obtained by accurate operation of the Signal Conditioning block to an output value of ± 1.2 volts.

Signal Conditioning of DC voltage inputs from ± 1V to ± 1000V full scale is accomplished by inserting appropriate attenuating factors for the selected full scale range. Signal conditioning in the 0.1V full scale range is accomplished in the A/D Converter block.

For AC voltage inputs, the Signal Conditioning block rectifies and filters the input signal so that the output, a DC signal, represents the average value of the sine wave multiplied by the conversion factor of 2.22 to yield the RMS equivalent (Figure 4-4).



Avg. value of half sine wave
(over a full cycle)

$$= \frac{1}{2\pi}\int_0^{\pi} A \sin\theta \, d\theta$$

$$= -\frac{A}{2\pi}\cos\theta\Big]_0^{\pi} = \frac{A}{\pi}$$

RMS value of Full Cycle
= 0.707 A

RMS = (π) (0.707) Avg. value
= (2.22) Avg. value

Figure 4-4 Derivation of RMS to AVERAGE Relationship

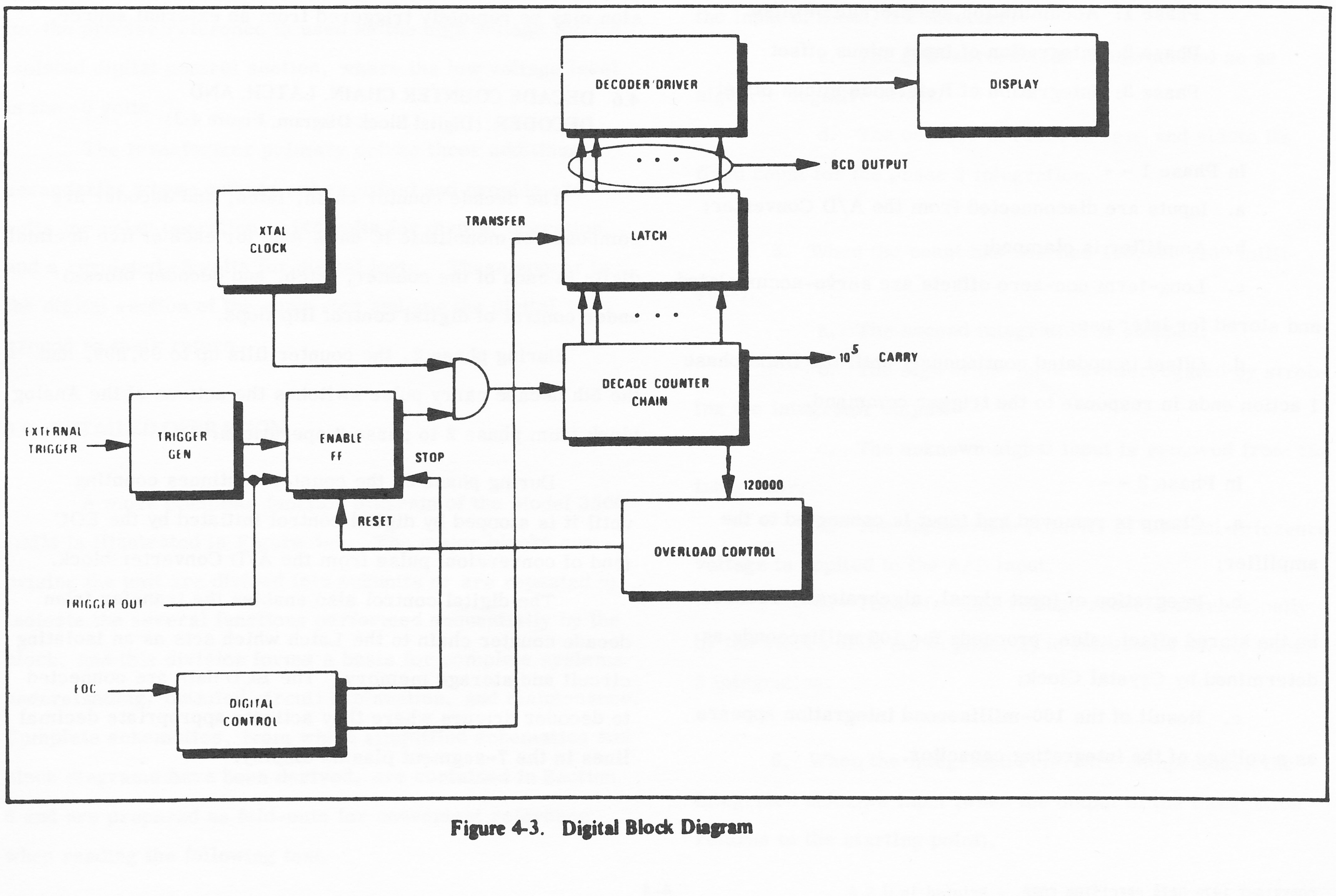

DECODER DRIVER
DISPLAY
BCD OUTPUT
XTAL CLOCK
TRANSFER
LATCH
DECADE COUNTER CHAIN
10^5 CARRY
EXTERNAL TRIGGER
TRIGGER GEN
ENABLE FF
STOP
RESET
120000
OVERLOAD CONTROL
TRIGGER OUT
EOC
DIGITAL CONTROL

Figure 4-3. Digital Block Diagram

In the Ratiohmic^{TM} resistance measurement technique, a voltage is connected across a range-selected accurately calibrated resistance in series with the unknown resistance, and the voltage drop across the unknown resistance is treated as an unknown DC voltage to be measured as before. In phase 3, however, the voltage drop across the calibrated resistance is used as the reference. Because the unknown and standard resistors are in series, the ratio of voltage drops is a direct measure of unknown resistance.

Attenuation components in the Signal Conditioning block are relay operated in response to control signals. These may be initiated by operating the front panel push buttons at the DMM, by control signals transmitted from a remote station via the rear panel connector, or by control signals generated within the DMM when in AUTO ranging.

4.4 TRI-PHASIC A/D CONVERTER BLOCK DIAGRAM (Figure 4-2)

The three phases of performance of the TRI-PHASIC A/D Converter are:

Phase 1: Accumulation and storage of offset
Phase 2: Integration of Input minus offset
Phase 3: Integration of Reference minus offset

In Phase 1 - -

a. Inputs are disconnected from the A/D Converter;

b. Amplifier is clamped;

c. Long-term non-zero offsets are servo-accumulated and stored for later use;

d. Offset is updated continuously until the DMM phase 1 action ends in response to the trigger command.

In Phase 2 - -

a. Clamp is removed and input is connected to the amplifier;

b. Integration of input signal, algebraically reduced by the stored offset value, proceeds for 100 milliseconds as determined by Crystal Clock;

c. Result of the 100-millisecond integration appears as a voltage of the integrating capacitor.

In Phase 3 - -

a. Input is disconnected from A/D;

b. Voltage of opposite polarity is selected from ISO-Polar reference, algebraically reduced by value of stored offset, and the difference integrated to discharge the integrating capacitor linearly to zero;

c. At the zero crossover, end of conversion is generated, and transmitted to digital control circuitry.

4.5 TRIGGER GENERATOR AND CLOCK (Digital Block Diagram, Figure 4-3)

Primary control for DMM measurement is the trigger which initiates each conversion (start of phase 2). The trigger, in its internal DMM circuitry, is generated by the discharge of a capacitor after an RC path charges a capacitor to a unijunction transistor break-down voltage. The trigger is factory selected for a pulse repetition rate of approximately 3 per second.

The trigger may be blocked and a conversion cycle delayed indefinitely by grounding the ENABLE input for as long as desired. The display, or BCD equivalent, is held until a new trigger is generated. In addition, each conversion may be remotely triggered from an external source.

4.6 DECADE COUNTER CHAIN, LATCH, AND DECODER. (Digital Block Diagram, Figure 4-3)

The decade counter chain, latch, and decoder are composed of monolithic IC units (one for each of five decimal digits in each of the counter, latch, and decoder blocks) under control of digital control flip flops.

During phase 2, the counter fills up to 99,999, and the 5th decade carry pulse switches the actions of the Analog block from phase 2 to phase 3 operations.

During phase 3, the counter continues counting until it is stopped by digital control initiated by the EOC (end of conversion) pulse from the A/D Converter block.

The digital control also enables the transfer from decade counter chain to the Latch which acts as an isolating circuit and storage memory. The BCD data are connected to decoder drivers where they activate appropriate decimal lines in the 7-segment plasma display.

4.7 RANGING (Digital Block Diagram)

Range scaling is accomplished by relays which may be activated in any one of three ways:

a. Manually - by pushing front panel range select push buttons;

b. Automatically - by logic control;

c. Remotely - when in remote trigger control, a discrete range scale may be selected, by grounding directly, or by a logic low level command.

4.8 POWER SUPPLY BLOCK

The Power Supply block may be connected for either a 115-volt or 230-volt AC Source of frequency from 47 to 63 Hz. The block is essentially two separate sets of supplies, driven from the same input transformer primary. The analog supply is triple shielded, floating, and incorporated in a "guarded" area for proper isolation. It develops ± 15V regulated supply voltage for the analog circuitry, -5V for the digital control in this section, and develops the 6.2 volt, oven controlled, extremely low temperature coefficient, reference source for the A/D Converter. Common ground for the precise reference is used as the high voltage for the isolated digital control section, where the low voltage level is the -5 volts.

The transformer primary drives three additional secondaries whose outputs are rectified and provide +20 volts for relay operation, +180 volts for display operation, and a regulated +5 volts for digital logic. These appear in the digital section of the converter and use the digital ground as their return.

4.9 DETAILED OPERATION

A more complete function diagram of the Model 3500 DMM is illustrated in Figure 4-5. The major blocks comprising the unit are divided into subunits or are repeated to indicate the several functions performed sequentially by the block, and this division forms a basis for complete systems understanding, detailed circuit explanation, and maintenance. Complete schematics, from which simplified schematics and block diagrams have been derived, are contained in Section 6 and are prepared as fold-outs for convenient reference when reading the following text.

The sequence of functions illustrated in Figure 4-5 consists of the following:

1. Measuring Mode and Range are selected. Proper attenuation elements for the selected range are connected in the Signal Conditioning block, and in the pre-amplifier block.

2. Input signal is applied.

3. Prior to the trigger pulse starting a conversion measurement, the A/D Converter input is clamped, and the Signal Conditioning output is removed from the A/D Converter. During that time, phase 1 drift integration proceeds and the self zeroing circuit determines the A/D amplifier accumulated drift and stores it for phase 2 and phase 3 operation.

4. Following the trigger pulse generated in the Timing & Control unit;

a. The clamp is removed from the A/D Converter.

b. The Signal Conditioner Output is connected to the input of the A/D Converter.

c. The self-zeroed drift is introduced as an algebric negative offset.

d. The counter is reset to zero and starts its fixed count for the phase 2 integration.

5. When the count has reached 100,000 (100 millisec.),

a. The second integration is stopped.

b. The sign of the input is interrogated by strobing the integrator output.

c. The unknown signal input is removed from the integrator.

d. The appropriate polarity of internal reference voltage is applied to the A/D input.

e. The reference voltage reduced algebraically by the stored drift (as in phase 2) is integrated during phase 3 integration.

6. When the integrated reference compensates the integrated unknown input (when the output of the integration returns to the starting point),

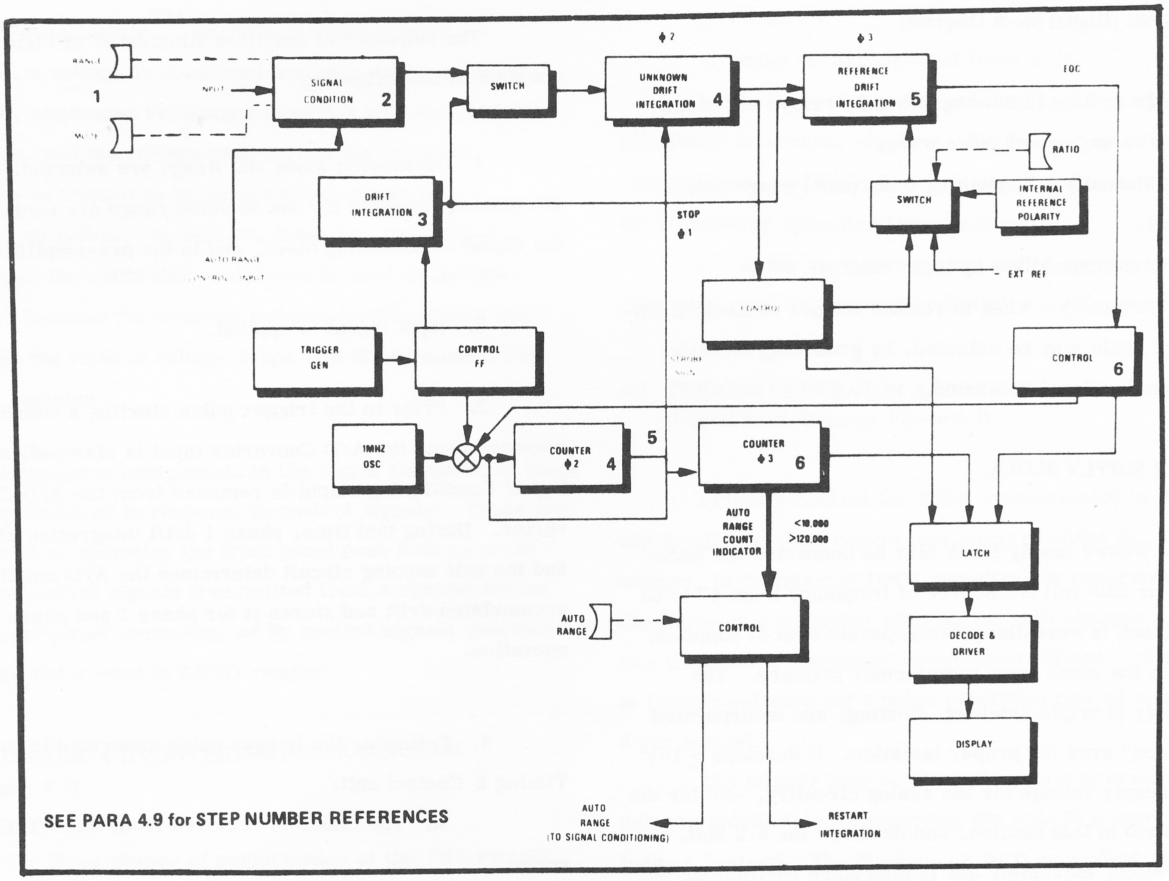

RANGE
1
INPUT
MODE
SIGNAL CONDITION 2
SWITCH
ϕ 2
UNKNOWN DRIFT INTEGRATION 4
ϕ 3
REFERENCE DRIFT INTEGRATION 5
EOC
RATIO
DRIFT INTEGRATION 3
SWITCH
INTERNAL REFERENCE POLARITY
AUTO RANGE CONTROL INPUT
STOP
ϕ 1
EXT REF
CONTROL
TRIGGER GEN
CONTROL FF
STROBE SIGN
CONTROL 6
1MHZ OSC
COUNTER ϕ 2 4
5
COUNTER ϕ 3 6
AUTO RANGE COUNT INDICATOR
<10,000
>120,000
LATCH
AUTO RANGE
CONTROL
DECODE & DRIVER
DISPLAY
SEE PARA 4.9 for STEP NUMBER REFERENCES
AUTO RANGE (TO SIGNAL CONDITIONING)
RESTART INTEGRATION

Figure 4-5 Model 3500 Functional System Block Schematic

a. Phase 3 integration process ends.

b. The input clamp is reestablished.

c. The clock input to the counter is stopped.

d. A READ OUT signal is transmitted indicating End of Conversion.

e. The accumulated count is transferred to the display.

The timing sequence is illustrated in the chart of Figure 4-6, indicating the three phases of the operation.

Detailed explanations of these functions are presented in the following sequence:

a. Input signal conditioning (Figure 4-5A)

b. Phase 1 Drift Integration

c. Phase 2 Unknown-Drift Integration (Figure 4-5C)

d. Phase 3 REFERENCE-DRIFT Integration (Figure 4-5D)

e. Digital Control and Display (Figure 4-5E)

f. Ranging circuits and Remote display and control functions.

4.10 SIGNAL CONDITIONING DETAILS

a. DC VOLTAGE

Input DC voltages are applied through the HI and LO input terminal, and connected to the input attenuator network through the contacts of Mode Switch S12 and S13 when placed in DC Volts Mode. Replay actions of K1 and K2, determined by the range selection, then establish the attenuator actions.

A simplified schematic of the DC Voltage signal Conditioning action is shown in Figure 4-7.

The relay pair (K1A and K1B) and relay K2A provide four range selections from 1V Full Scale to 1000V Full Scale. (Range change from 1.0V to 0.1V Full Scale is accomplished in the A/D Converter.) Action of the relays and resultant attenuation of the input signal on the different range scales are summarized by the table below.

Full Scale Range Select	Relay K1 1/100	Relay K2 1/10	Result. Atten.
1 Volt	OFF	OFF	1
10 Volts	OFF	ON	1/10
100 Volts	ON	OFF	1/100
1000 Volts	ON	ON	1/1000

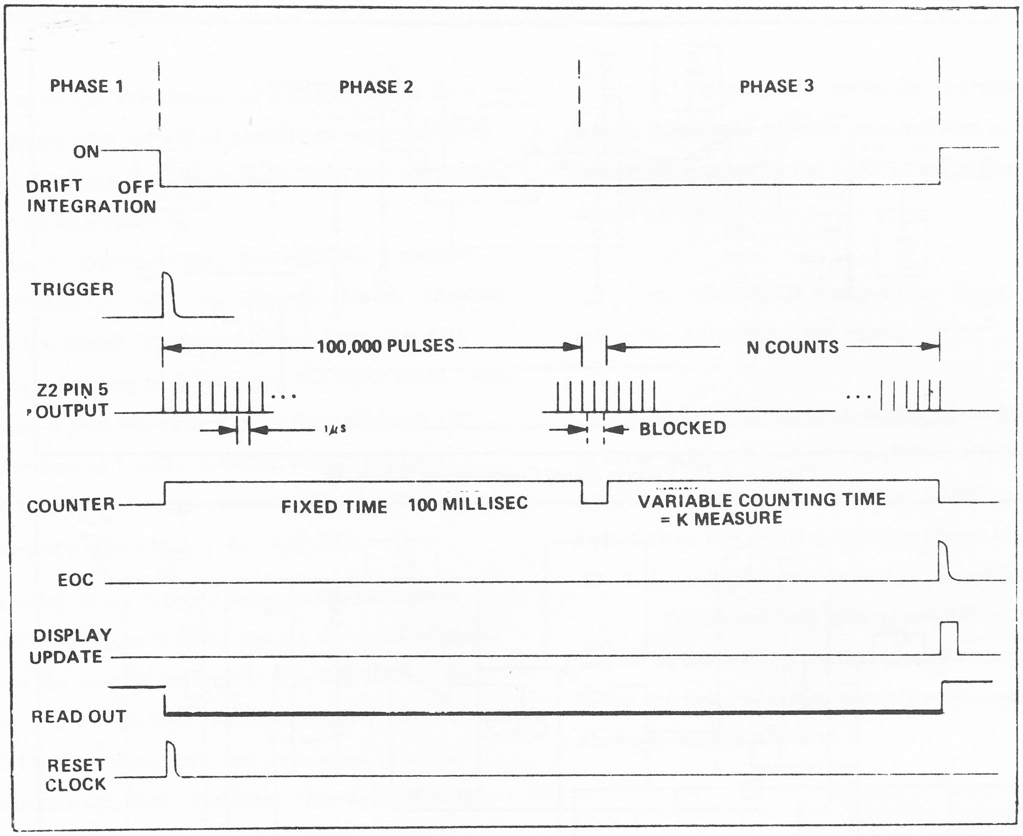


Figure 4-6 Tr-Phasic logic and control waveforms.

Full scale voltage delivered to the A/D Converter is 1 volt on all ranges except the 0.1 Volt scale. In that range the full scale output of the Signal Conditioning block is 0.1 volt. In all cases, overrange values, up to 120% of full scale are converted accurately in the A/D Converter, up to a maximum input of 1000 volts DC.

The signal conditioner amplifier is a high impedance, unity gain, isolation unit, provided with voltage and current offset adjustments. It is connected only when relay K2 is activiated. The input network, including R121 and R117 and the biasing diodes, is designed to protect the Multimeter from accidental connection of high voltages up to ± 1000 volts regardless of the range selector setting.

When not in DC Volt Measurement Mode, the input is removed from the indicated circuitry.

b. AC Voltage

In AC Voltage Mode, the input is connected to a broad band active attenuator followed by an active rectifier and filter. Networks in the feedback path of the input amplifier determine the attenuation for the selected full scale range. Capacitor trimmers are adjusted to maintain constant feedback ratios over the range of input signal frequencies. Manual push button action or automatic ranging signals control the relay-operated selection of the appropriate attenuation decade. A simplified schematic of the circuit is shown in Figure 4-8. This illustrates the amplifier Z26 and its feedback decades, the half-wave rectification of the second amplifier Z Z27 output, and the low pass filter R27, C26, which passes the average DC component of the rectified output.

The filtered, rectified DC Voltage output is thus scaled to the RMS value of the applied input signal and connected to A/D Converter via the switching circuit.

4.11 RATIOHMIC RESISTANCE INPUT CONDITIONING DETAILS

Connections for Resistance measurements are shown in the schematic of Figure 4-9. The unknown resistor R_X, is made part of a resistance series set consisting of a selected range scale resistor, R_S, the undetermined contact resistances Rc_1 and Rc_2, and itself. This set is driven from the temperature controlled +6.2V reference voltage.

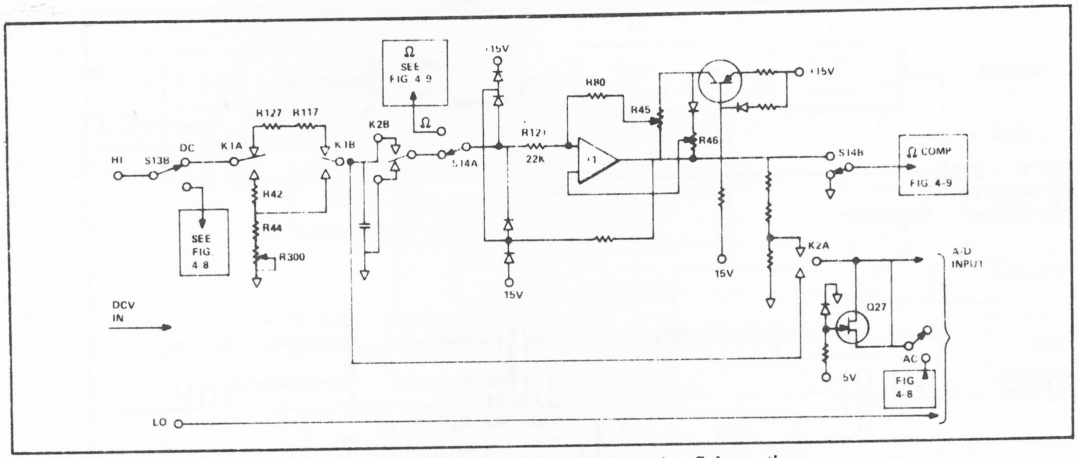

Ω
SEE
FIG 4-9
Ω
+15V
+15V
R80
R127
R117
K2B
R121
22K
R45
HI
S13B
DC
K1A
K1B
S14A
+1
R46
S14B
Ω COMP
FIG 4-9
R42
R44
SEE
FIG
4-8
R300
15V
15V
K2A
A/D
INPUT
Q27
DCV
IN
AC
5V
FIG
4-8
LO

Figure 4-7 DC Voltage Signal Conditioning Schematic

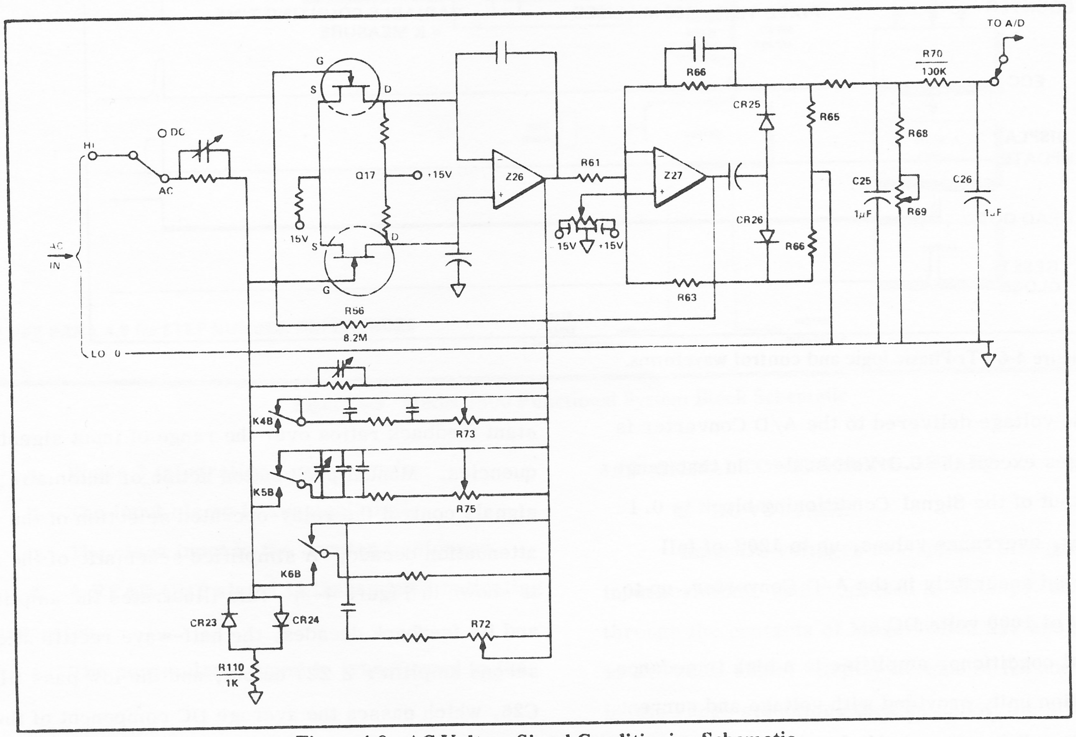

TO A/D
R70
130K
G
S
D
R66
CR25
R65
R68
DC
HI
AC
Q17
+15V
Z26
R61
Z27
C25
1μF
R69
C26
1μF
15V
S
D
CR26
R66
AC
IN
15V
+15V
G
R63
R56
8.2M
LO
K4B
R73
K5B
R75
K6B
CR23
CR24
R72
R110
1K

Figure 4-8 AC Voltage Signal Conditioning Schematic

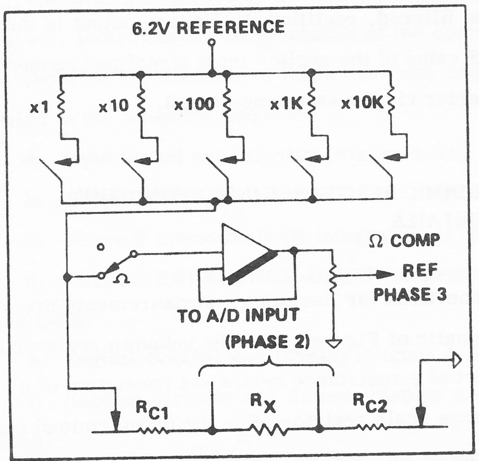

6.2V REFERENCE
x1
x10
x100
x1K
x10K
Ω
Ω COMP
REF
PHASE 3
TO A/D INPUT
(PHASE 2)
R_{C1}
R_X
R_{C2}

Figure 4-9 Resistance Measurement Signal Conditioning

During phase 2, the voltage drop across Rx is connected to the A/D Converter where it is processed in the same manner as a DC input signal. During phase 3, the voltage drop across the selected range scale resistor is buffered by the unity gain amplifier, divided by 6.2 using the calibrated divider network, and connected to the converter as the Reference input.

The indicated circuit operation features the following:

a. The same current develops the unknown and reference voltage signals.

b. The contact resistance voltage drops do not affect performance.

4.12 A/D CONVERTER DETAILS

Operation of the Tri-Phasic A/D Converter in its 3 phases is described with the aid of simplified schematics of Figure 4-10A and Figure 4-10B, derived from the complete reference drawing in Section 6.

Referring to Figure 4-10A, during phase 1 switch Q1 is open, switches Q2, Q23, and Q25 are closed. Opening of Q1 removes the Signal Conditioned input from the A/D preamplifier A1. Closing of Q2 clamps the input to A1, and, with Q23, closes a path whereby C34 is charged from the ISO-Polar reference to 1 volt. Closing of Q25 permits capacitor C36 to store a charge compensating for the accumulated non-zero offset in A1, A2, and Z29.

Appearance of the trigger pulse in the secondary of transformer T2 (Figure 4-10B) signals the start of phase 2, and initiates the control actions by flip flop Z31A. The trigger causes pin 5 to go high and consequently Q1 to close. The output Z31B pin 8 goes low, and consequently opens transistor switches Q2, Q23, and Q25. The actions of Q3 and Q4 are determined by the selection of 1V or .1V range.

a. Opening Q23 opens the charging path to C34 (Figure 4-10A) and leaves C34 charged to 1 volt and isolated during phase 2.

b. Opening Q25 opens the charging path of C36 and leaves it charged with the accumulated compensation for zero drift applied to the input of the differential integrating amplifier A2.

c. Closing Q1 connects the Signal Conditioned output to the A/D Converter input.

Phase 2 integration action takes place in the chain of three active elements: amplifier A1, amplifier A2, and amplifier Z29. Amplifier A1 is a high gain, high input impedance, low offset amplifier whose feedback resistors R9, R10, and R15 determine the closed loop gain.

The closed loop gain of amplifier A1 is either 8 or 80 depending upon the condition of switches Q3 and Q4, and these are determined by the full scale range selection as shown in the table below.

F.S.R. Select	Q3	Q4	AMP Gain	
			Ø2	Ø3
Not .1	0	1	8	8
.1	$\overline{Ø3}$	$\overline{Ø2}$	80	8

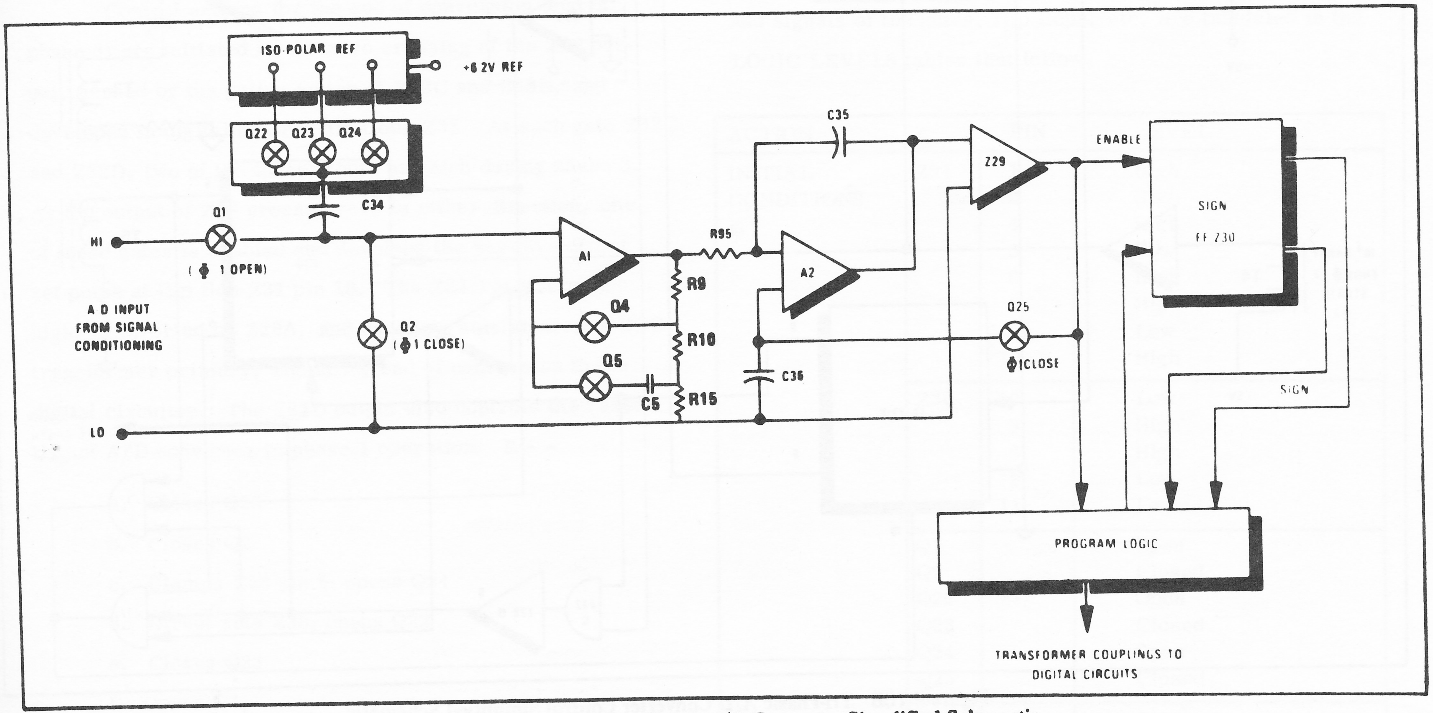


Figure 4-10A Tri-Phasic A/D Converter Simplified Schematic

As indicated in the table above, the amplifier gain is 8 for both signal input integration and for reference input integration for all range scales except .1. On the .1 range scale, the gain is changed by a factor of 10 from ø2 integration (signal input) to ø3 integration (reference input). Thus, a 0.1 volt full scale input is conditioned to the 1V full scale so that the precision reference and voltage need not be changed. The values of R9, R10, and R15 accomplishing this scale factor change are 7.1 5K, 900, and 100 ohms, respectively.

The function of C5 is to maintain the amplifier offset in the circuit through the switching action.

The output of amplifier A1 is one input to integrating amplifier A2 whose integration constant is determined by C35 and R95. The other input to amplifier A2 is the voltage on C36, the stored value of the voltage compensating for the accumulated zero offset dervied in phase 1.

Output of amplifier A2 drives high gain amplifier Z29 to saturation during phase 2. Its output polarity is used to indicate the sign of the unknown input.

Phase 2 integration proceeds until the appearance across the secondary of T4 of a positive-going pulse signalling a 10^5 carry from the digital block. This now appears as a negative pulse clocking flip flop Z30A pin 2 and as a direct set for flip flop Z31A (pin 4). The resulting actions controlled by these flip flops initiate the phase 3 operation of the A/D Converter.

The output, pin 5, of Z31A, which had been high from the start of phase 2, now goes low, opening Q1, and thereby removing the signal input from the A/D amplifier. Action of flip flop Z30A in response to the clocking pulse depends upon its input conditions just prior to receiving that pulse. This in turn was determined by the output of amplifier Z29 during phase 2. Amplifier Z29 was driven to saturation in the positive or negative direction corresponding to the sign of the input signal.

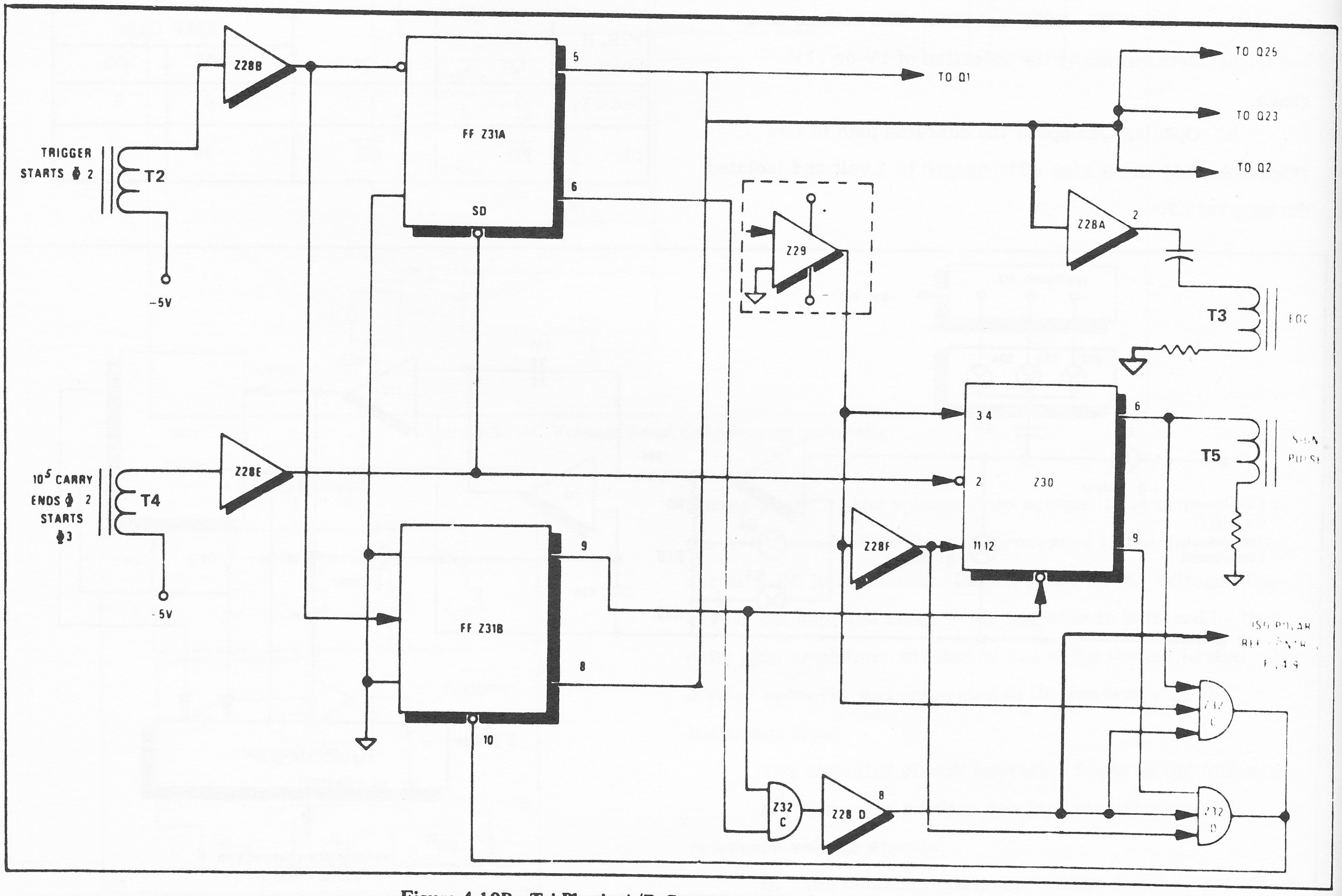


Figure 4-10B Tri-Phasic A/D Converter Control Simplified Schematic

If the input signal had been positive, Z30A pin 11 would have been low and the clocking pulse would not have changed the high level at pin 6, thus producing no pulse across the primary of "sign" pulse transformer L5. If the input signal had been negative, Z30A pin 11 would have been high and the clocking pulse would cause Z30A pin 6 to go low producing a pulse across the transformer T5 primary and transmitting a negative sign indication to the Digital circuitry. The voltage level deveoped by flip flop Z30 at pin 9 controls the sign of the reference signal to be switched to the amplifier input at the start of phase 3. (Refer to Figure 4-11 in conjunction with Figure 4-10B.)

During phase 2, both Q22 and Q24 are open. The low level output at Z30 pin 9 had kept Q22 open; and the output of Z28 pin 6 had been clamped low through CR28 to Z28D, keeping Q24 open. If the input signal had been positive, Z30 pin 9 would have remained low, keeping Q22 open. The carry pulse control action removes the clamp on the Z28 pin 6 output permitting the output of Z28 pin 6 to go high, closing Q24. This action places the high side of C34 at reference zero potential and negative one volt at the A/D amplifier input. If the input signal had been negative, Z30 pin 9 would go high, closing Q22 and connecting the high side of C34to reference+2V causing a positive one volt at the A/D amplifier input.

Control actions for the end of conversion (end of phase 3) are initiated by the zero crossing of the Z29 output, sensed by the gating action of Z32C and Z32D, and developed in digital control flip flops Z31. At each gate Z32C and Z32D, two of the three inputs are high during phase 3. As the output of Z29 crosses zero in either direction, one of these gates is enabled and develops the negative direct set pulse at flip flop Z31 pin 10. The Z31D output goes high, is inverted by Z28A, and develops a pulse across EOC transformer primary, signalling end of conversion to the digital circuitry. The Z31D output also controls the resetting of A/D converter to phase 1 operation. It - -

a. Closes Q25
b. Closes Q2
c. Clamps Z28 pin 6; opens Q24
d. Direct sets Z30; opens Q22
e. Closes Q23
f. Opens Q1.

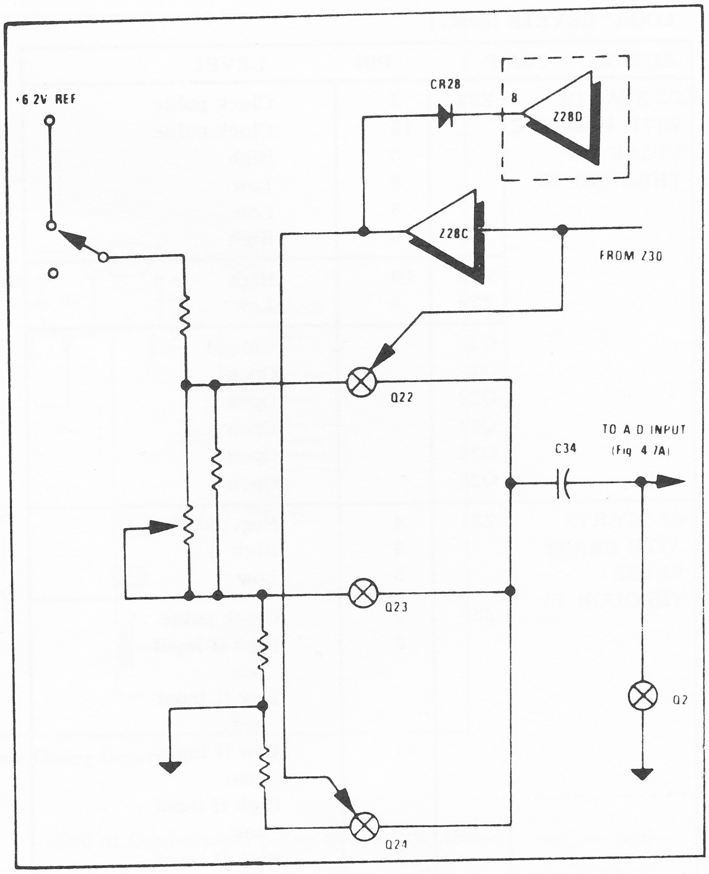


Figure 4-11 ISO-Polar Reference Switching Simplified Schematic

In summarizing the actions of the A/D converter circuitry during the three phases of operation, the levels and signals of the gates, flip flops, etc. are tabulated in the LOGIC LEVELS tables that follow.

ACTION	Z	PIN	LEVEL
INITIAL CONDITIONS Ø1	Z31	1	High
		2	High
		4	High
		5	Low
		6	High
		8	High
		9	Low
		10	High
	Z30	10	Low
		3	High
		6	High
		9	Low
		11	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
	Z28	8	Low

LOGIC LEVELS (cont.)

ACTION	COMP	PIN	LEVEL
Ø2 STARTS WITH POSITIVE PULSE THROUGH T2	Z31	1	Clock pulse
		13	Clock pulse
		5	High
		6	Low
		8	Low
		9	High
	Z30	10	High
	Z28	8	Low
	Q1		Closed
	Q2		Open
	Q22		Open
	Q23		Open
	Q24		Open
	Q25		Open
Ø3 STARTS WITH CARRY PULSE THROUGH T4	Z31	4	Neg. pulse
		6	High
		5	Low
	Z30	2	Clock pulse
		3	High if input pos. Low if input neg.
		11	Low if input pos. High if input neg.
		6	High if input pos. Low if input pos.
		9	High if input neg. Low if input neg.
	T5		Pulse if input neg. No pulse if input pos.
	Z28	8	High
	Q1		Open
	Q2		Open
	Q22		Closed if input neg. Open if input pos.
	Q23		Open
	Q24		Open if input neg. Closed if input pos.
	Q25		Open
END OF Ø3; Z29 PIN 7 CROSSES ZERO	Z32	6 or 8	Goes Neg. pulse
	Z31	10	Low
		8	High
		9	Low
END OF CONVERSION; NEGATIVE PULSE THROUGH T3	Z30	10	Low
		6	High
		9	Low
	Z32	8	High
		6	High
	Z28	8	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
RETURNING TO Ø1 OPERATION			

4.13 TRIGGER GENERATOR AND COUNTER

a. Trigger Generation

The trigger pulse initiating each conversion process may originate either from an external source or from internal circuitry shown in the simplified form of Figure 4-12. Capacitor C1 charges toward +5V through R15 until the firing voltage of Q40 is reached. A pulse approximately 100 μsec wide and 4 volts magnitude is developed across R16 and connected to J input of the control flip flop (Z2 pin 2). The sawtooth charge-discharge singal and the resulting trigger timing signal waveforms are shown in Figure 4-12.

The trigger control signal is inverted through Z21-, and then is gated through Z21- External input at terminal J, ENABLE, is normally high, permitting the internally generated trigger signal to be gated to flip-flop Z2A, where it is connected to the J terminal as a high logic level input.

Flip-flop Z2A, which has been reset by the end of conversion pulse, will have a low level on output pin 5 and a high level on pin 6. At the first clock pulse after the trigger, Z2A transfers the high J input level to the output, pin 5, which then enables gate Z3B and transmits succeeding clock pulses through to the counter chain. Z2A pin 6 goes low at the same time and, through inverter Z1-12 generates a counter reset pulse. An invested reset pulse is used to reset the under-and over-range flip-flops Z20A and Z20B.

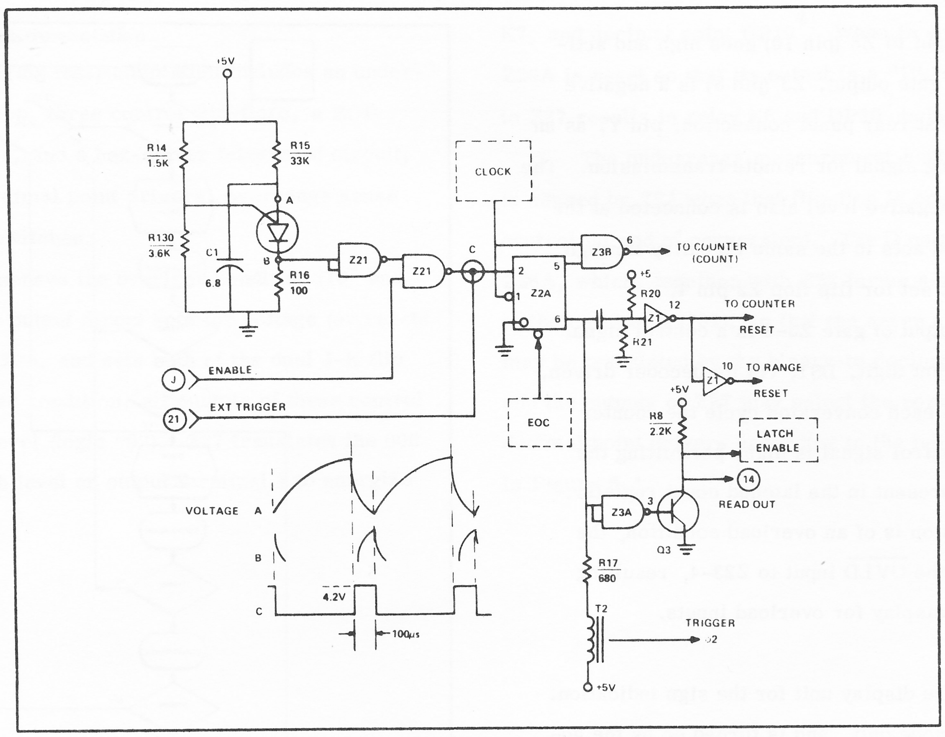


Figure 4–12 Trigger and Timing Generator

The low level on pin 6 of Z2A also transmits a pulse through transformers T2, to initiate phase 2 of the triphasic conversion cycle.

After inversion through Z3 pin 3, transistor Q3 conducts; its collector goes low, isolating the latching circuit from the counter. The latch and display retain the stored count until the next conversion update, and an output signal, READOUT, is available at the rear panel connector to indicate this event in the cycle. This is a High (T^2L/DTL) output level between conversions.

The leading edge of the negative going waveform is differentiated (C5, CR20, and R21) as the input to Z1 (pin 12), inverted, and generates a positive going pulse to reset the decade counter IC's, Z4 through Z8.

The inverted counter reset pulse, at the output of Z1 (pin 10) presets the range control flip flops Z20 pin 10 and pin 4, and Z2 pin 10.

b. Counter Chain (Figure 4-12)

The crystal-controlled clock is a series-mode crystal circuit consisting of crystal Y1 and inverter Z1. It develops 1 MHz pulses which are gated into the counter during phases 2 and 3. The counter registers accumulate the count during phases 2 and 3 until receipt of the EOC (End of Conversion) pulse at the EOC transformer secondary. This resets flip flop Z2A, and pin 5 goes low, blocking the timing pulses at gate Z3 5-6. Simultaneously, Z2 pin 6 goes high cutting off Q5, collector voltage goes high, permitting the count in Z4-Z8 and Z2B to be transferred to the latches, and through them to the decoding and display driving registers Z15 and Z19.

Outputs of the counter chain are transferred through the latching registers as BCD data. These are immediately available at the tab connector of the DMM rear panel for remote display or control purposes. In the DMM, the decoding registers Z15 through Z19 convert BCD to decimal signals.

If the DMM is in a manual range selection, and the developed count in phase 3 is less than 120,000, the conversion cycle is complete.

c. Overload

If an end of conversion pulse is not received during phase 3 by the time the counter reaches 120,000 (a display of 120,000), an OVERLOAD condition exists, and this event is sensed at gate Z3. One input to Z3 (pin 9) is set at a high level by the toggled output of Z20 pin 5 when the count reaches 10^5 in phase 3. When the counter reaches

20000, the second input to Z8 (pin 10) goes high and activates the gate. The gate output, Z3 (pin 8) is a negative waveform, available at rear panel connection, pin Y, as an OVERLOAD indicating signal for remote transmission. The overload indicating negative level also is connected at the output of Z1 pin 2 and acts in the same circuitry through Z11 pin 2 as a direct set for flip flop Z2 pin 4.

The OVLD output of gate Z3-8 is a control signal for the most significant digit, DS1, via its decoder driven, Z23. At the start of each conversion cycle the counter is reset, and this control signal is high, permitting the "1" to be lighted if present in the latched count register. Then, if the conversion is of an overload condition, the "1" is turned off by the $\overline{\text{OVLD}}$ input to Z23-4, resulting in the blinking MSD display for overload inputs.

d. Sign

DS1 is also the display unit for the sign indication. It is enabled in DC mode only, and is turned on by the action of the sign pulse transformer T5 via latch flip flops Z14. It is strobed into the first latch at carry pulse and transferred to second latch at EOC.

4.14 RANGING

4.14.1 General

As shown in Figure 6-4, all range scale selections are controlled by the actions of Relays K1 through K7, and decimal point selection is slaved to the relay action. Each relay activation is controlled by drivers contained in integrated circuit Z34, and they, in turn, may be controlled either by the operation of the automatic ranging digital logic, or by the manual operation of front-panel push buttons or remote signals. Signals controlling the relay drivers simultaneously operate the appropriate transistor control of the displayed decimal point.

Figure 6-4 also includes a matrix chart relating the states of the relays for each selected range scale. It also includes the necessary states of the 3 auto range flip-flops for the same results.

4.14.2 Auto-Ranging

The auto-ranging logic responds to the measured input when less than 10000 counts or more than 120000 counts according to the logic flow shown in Figure 4-13.

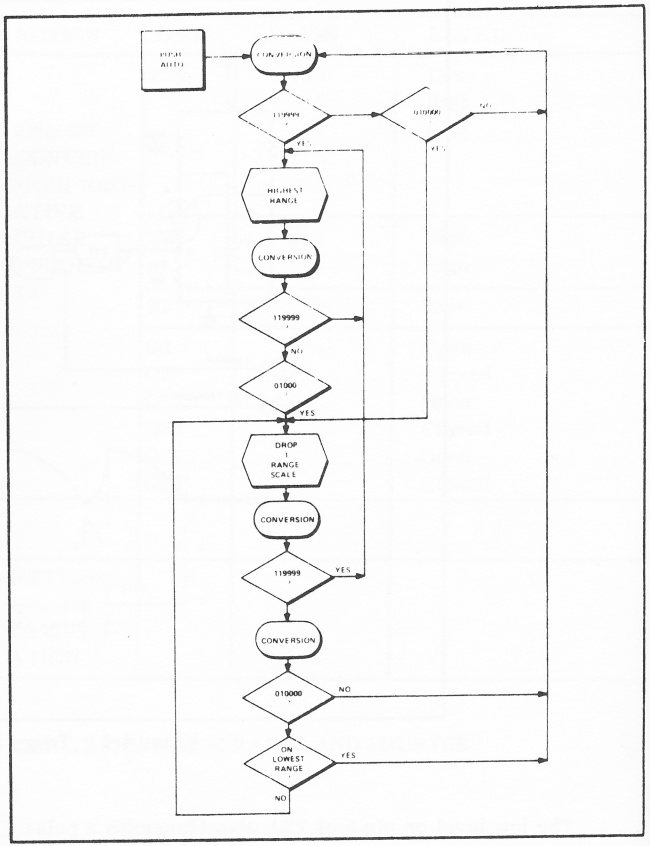


Figure 4-13 Auto-Ranging Control Logic Schematic

After the AUTO push button is operated, each conversion is sensed by the DMM circuitry, which responds as shown in Figure 4-13, and as described below.

a. At any time that a value greater than 119999 counts is sensed, the cricuitry switches the meter to the highest range (1K for voltage, 10K for ohms) for the next conversion.

b. If, after switching to the highest range, the next conversion measures a value less than 10000, this underrange condition is sensed, and the circuitry drops the range scale to the next lower range.

c. Thereafter, two successive underrange conversions are required before the range scale is changed to the next lower one.

d. Lower range scales are switched in until the lowest scale has been selected.

e. An overrange sensing causes a highest range scale selection at any time it is sensed.

4.14.3 Auto Ranging Instrumentation

The auto ranging instrumentation includes an underrange storage flip flop, three control flip-flops, a BCD to decimal converter, and a hex-driver integrated circuit, in addition to the decimal point drivers, overrange sense gates, and manual switches.

Gate Z21-3 senses the overload condition (10^5 and 2×10^4 inputs). Its output direct sets for voltage (or resets for ohms) flip-flop Z26, and sets both of the dual J-K flip Z22. In the overload condition, all outputs of these control flip-flops are low level (logic "0"). Z27 translates the 000 input to place a high level on output terminal 1 to energize K7, and decimal point $DP10^4$. When in voltage measurement Z26A is reset so that its output is a "1", and the 100 input to Z27 results in relay K6 and $DP10^3$ being activated.

The underrange measurement (under 10000 counts) is sensed by Z24 when that flip-flop is enabled by the $\overline{READ}$ control (at end of conversion). The Q output of Z24 toggles Z26A, which, together with Z22 forms a binary counter up to the count of 6 (101), so that the seven states 000 to 101 may be translated by the binary-to decimal decoder Z27, and the outputs of Z27 may select the correct relays and decimal point drivers according to the tabular array included in Figure 6-4.

Chapter 5

MAINTENANCE

5.1 GENERAL

Model 3500 Digital Multimeter uses solid state components and integrated circuits (except for display tubes), and are designed for reliable long-life operation. Except for calibration verification, no operator maintenance should be required, and there should be no normal requirement for opening the DMM case. Should any malfunction require corrective action within the warranty period, arrangements should be made to obtain factory assistance.

CAUTION

Data Precision provides this maintenance information primarily for users of Model 3500 Digital Multimeters in need of repair after the expiration of the Warranty period. The information is intended for users who are qualified and competent to effect any needed repairs. The equipment may be returned for repairs at a nominal fee if the user should elect to have the factory make repairs.

Should the qualified user attempt to troubleshoot and repair the DMM, he will find that Model 3500 DMM contains a number of features especially designed for simplified unambiguous troubleshooting and fault indication. Among these are:

a. Full and complete design and parts data in this Instruction Manual;

b. A positive troubleshooting procedure intended for effective use by competent technical personnel in isolating and correcting all but the most subtle and intricate problem sources;

c. Mechanical parts layout and identification for logical and easy location.

5.2 PARTS GROUPING AND THE TEST STAND-OFF GRID

The printed circuit board is etched to show the grouping into major functions of the components (Figure 5-1). These correspond, genrally, to the schematics in Section 6. The separate groups are individually named, the designations appearing along the edge of the board. When the Guard Shield is removed, the floating Analog power supply and the analog portion of the A/D Converter and Signal Conditioner are revealed. The two amplifiers of the A/D Converter and the CLAMP/UNCLAMP switching module are separate modular components. They are mounted on the base PC board as integral component assemblies.

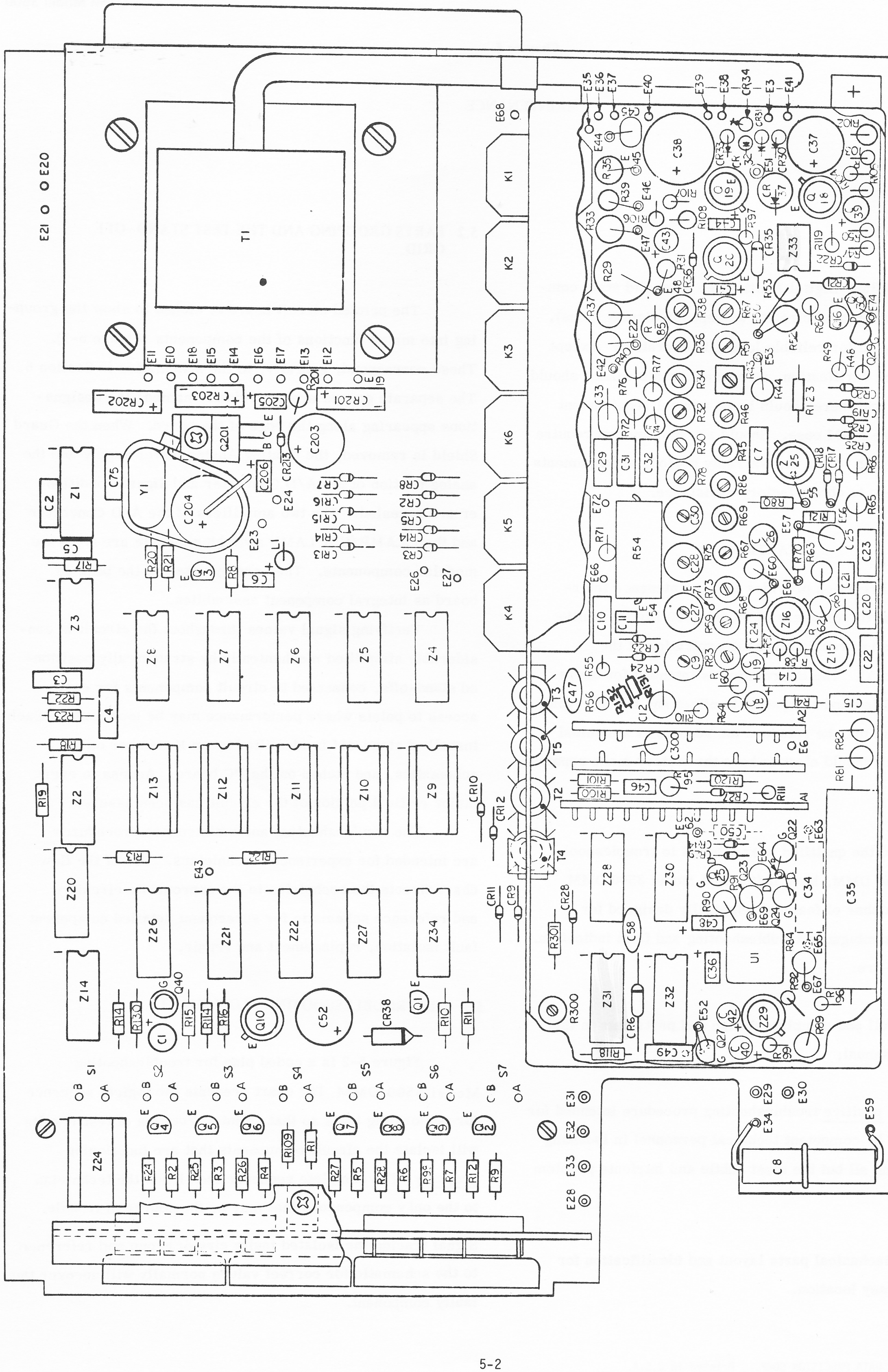
Verifying signal values throughout the circuit is considerably simplified mechanically by strategically positioned stand-offs, connected to circuit components for easy access to points where performance may be monitored. Each installed stand-off is identified by an E-number on the schematics, and etched on the PC board. Access to every major critical portion of the circuit has been assured.

The troubleshooting and maintenance procedures are intended for experienced technicians. Use of the flow chart directs the technician to the appropriate circuitry and reference schematic for subsequent detailed component fault isolation, replacement and repair.

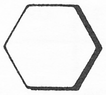
5.3 THE TROUBLESHOOTING FLOW CHART

Figure 5-2 is a coded plan for troubleshooting Model 3500 DMM. The chart presents the logical sequence for performing tests so that an interpretation of test results will isolate the circuit components that are functioning properly. The complete sequence then leads the technician to the only components that may be the source of trouble.

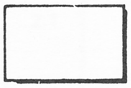
Signal tracing the isolated faulty circuit group and reference to the schematic for correct values normally will uncover the faulty component.


T1
E21
E20
K1
K2
K3
K6
K5
K4
E68
E11
E10
E18
E15
E14
E16
E17
E13
E12
E19
CR202
CR203
C205
CR201
R201
Q201
B C E
C203
CR213
C206
C204
Y1
C75
Z1
C2
C5
R17
R20
R21
Q3
R8
C6
L1
E23
E24
CR7
CR16
CR15
CR14
CR13
CR8
CR2
CR5
CR4
CR3
E26
E27
Z3
Z38
Z7
Z6
Z5
Z4
C3
R22
R23
C4
R18
R19
Z2
Z13
Z12
Z11
Z10
Z9
CR10
CR12
T3
T5
T2
T4
Z20
R13
R12
E43
Z26
Z21
Z22
Z27
Z34
CR11
CR9
CR28
R301
R300
Z14
R14
R130
C1
Q40
R15
R114
R16
Q10
C52
CR38
Q1
R10
R11
S1
S2
S3
S4
S5
S6
S7
Q4
Q5
Q6
Q7
Q8
Q9
Q2
Z24
R24
R2
R25
R3
R26
R4
R109
R1
R27
R5
R28
R6
R29
R7
R12
R9
E31
E32
E33
E28
E29
E30
E34
E59
C8
E35
E36
E37
E40
E39
E38
CR34
E3
E41
C45
C38
C37
CR31
CR33
CR32
CR30
E44
E51
R35
E45
R39
Q19
Q18
CR37
R102
R103
R33
E47
C43
R107
R108
C44
R97
Q20
CR35
Z33
R119
R29
R31
CR36
E48
R38
R47
E50
R53
E52
Q16
E74
R37
E22
R85
R36
R51
R52
R86
R49
R46
Q29
E42
R40
R77
R34
R43
E53
R44
R123
C33
R76
R72
R74
R32
R46
C29
C31
C32
R30
R78
R45
C7
Z25
CR18
CR17
R66
R80
R86
E55
E72
R71
R54
C30
R69
E57
R121
E56
R65
C28
R75
R67
C26
E60
R70
R63
C25
C23
E66
C10
C11
E54
C27
R73
R68
E61
C21
C20
R59
R83
Z16
R62
R57
C24
C9
CR24
CR23
C19
C47
R55
R132
R131
R160
R58
C14
Z15
C22
R56
C12
R110
R64
C18
R41
C15
A2
C300
E6
R82
R61
R101
C46
R95
R120
R100
CR27
R111
A1
Z28
Z30
E62
C50
Q22
E63
Q25
Q23
E64
R91
R90
C34
C35
C58
C48
Q24
E69
R84
E65
U1
C36
Z31
Z32
R92
E67
R96
CR6
E52
C42
Z29
R89
R118
C49
Q27
C40
R99
Figure 5-1. Parts and Stand-Off Layout on PC Board Assembly

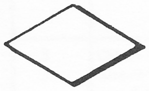
A standard graphic code has been used in the flow chart:



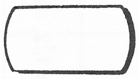
Set Up Instructions. Define input stimulus value and where applied.



Measure parameter (volts, amps, ohms)



Following measurement, evaluate for next path step



Remove and Replace if unique and unambiguous (Multiple source of malfunction possible)

5.4 USING THE TROUBLESHOOTING FLOW CHART

As shown in Figure 5-2, one starts by activating the POWER push button and checking to see if the Display comes ON. If not, the chart directs the maintenance man to perform Test No. 1 as defined in the integral Table of Tests. Test No. 1 calls for the measurement of a DC voltage between stand-offs E18 and E19, and checking for a nominal voltage of 180 volts. If the voltage is present, then, according to the chart, it is concluded that the display and its circuitry are in need of further fault isolation.

If the voltage check of Test No. 1 indicates an incorrect value of the DC voltage, then the chart directs the maintenance technician to use Reference Dwg. Sheet 5 and to measure the other output voltages in accordance with Tests 2.1 and 2.2. The Tables of Tests also indicate the driven circuits for each of the supply voltages. These may be the cause of incorrect voltage measurements when checking power supply elvels and should be checked for excessive current drains by examining driven components and their nearby components for signs of elevated temperatures. The reference drawing includes the pin identification of the components driven by each supply.

Continue through the flow charts as directed, and the successive steps will confirm the proper operation of incremental portions of the DMM as they contribute to the performance as a whole. An incorrect reading in any step identified the circuit components as a group within which the malfunction most probably originates.

The testing sequence represented by the charts beginning with Figure 5-2 is concluded with a calibration to complete the maintenance process. Complete DMM function will have been verified by this process, but only those coded outputs actually tested are verified. Any pattern of missing digits may not be detected in these tests, and such a symptom is indicative of a malfunctioning counter, latch, or decoder IC.

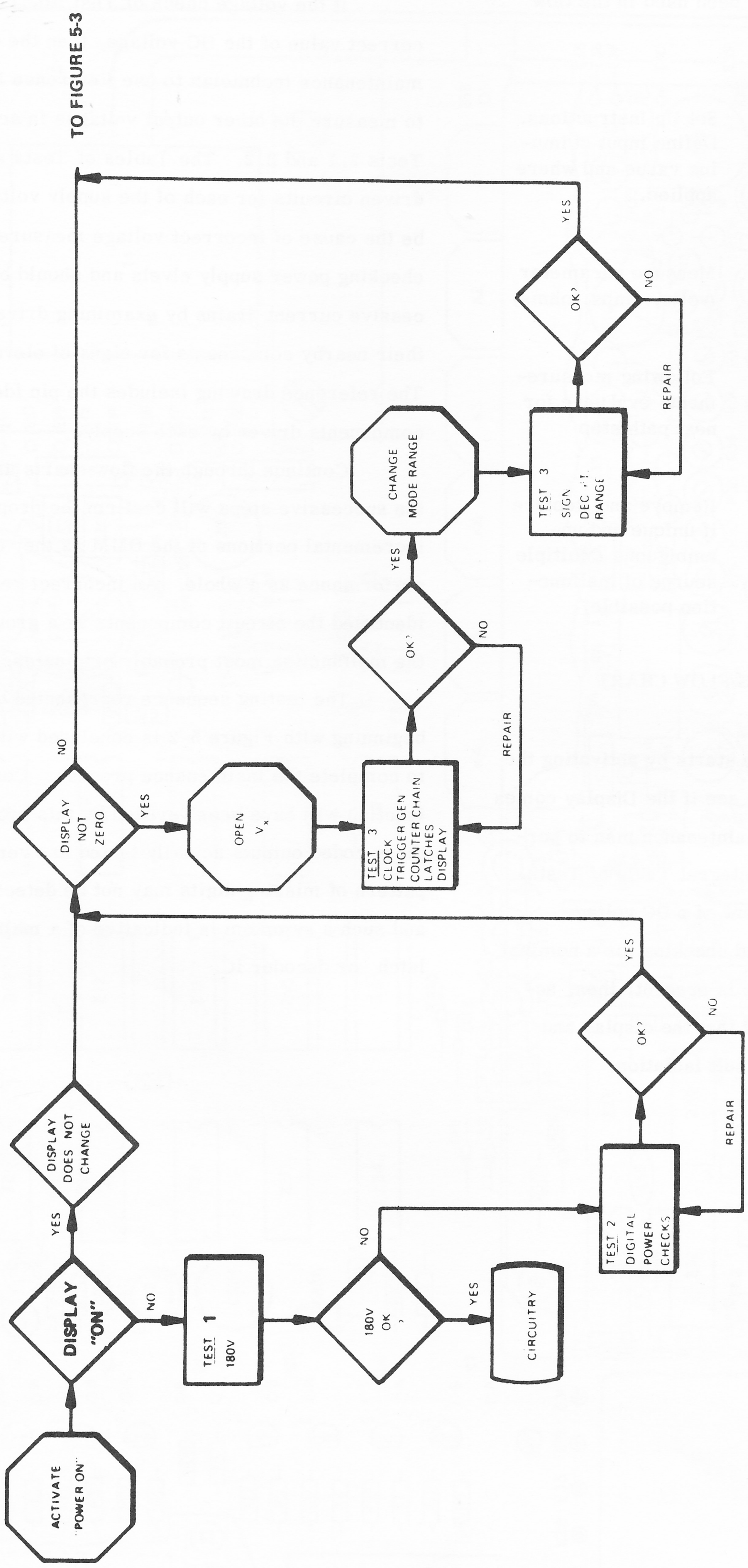

ACTIVATE "POWER ON"
DISPLAY "ON"
NO
YES
TEST 1 180V
180V OK ?
YES
CIRCUITRY
NO
TEST 2 DIGITAL POWER CHECKS
OK?
NO
REPAIR
YES
DISPLAY DOES NOT CHANGE
DISPLAY NOT ZERO
NO
YES
OPEN V_x
TEST 3 CLOCK TRIGGER GEN COUNTER CHAIN LATCHES DISPLAY
OK?
NO
REPAIR
YES
CHANGE MODE RANGE
TEST 3 SIGN DECIMAL RANGE
OK?
NO
REPAIR
YES
TO FIGURE 5-3

Figure 5-2 Trouble Shooting Sequence. Tests 1, 2, and 3.

Tests 1,2 and 3. See Figure 5-2.

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE*	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
1	Activate Power ON	DC Volts	E18: E19	+180V 198	± 10%	Power Supply Drawing SH5	DISPLAY Supply
2.1		DC Volts	E17: E19	+20V 19.1	18 to 22	Power Supply Drawing SH5	Relay Supply
2.2		DC Volts	E16: E19	+5V 4.67	4.5 to 5.5	Power Supply Drawing SH5	Digital Logic Supply
3	Open Vx Short Z1A pin 1 to GND						ϕ1, ϕ2, ϕ3; No EOC, 120000 Count
3.1		Frequency Count	Z2A pin 1	1 MHz	±1 kHz	Clock Circuit Drawing SH1	Clock
3.2		Waveform Analysis	Z2A-2	Amp >+2.5V Rep Rate ~3 pps	-0, 2.5 - 5.5	Trigger Gen Drawing SH1	Trigger Generator
3.3		Frequency	Z4 through Z8 and Z2 Pin 14 on each	1 MHz to 10 Hz (by 10) and 5 Hz	± 0.1%	Decade Counter Drawing SH1	Decade Counter Chain and Binary Counter
3.4		Logic Levels	Rear Conn DATA OUT Tabs	BCD for 120000		Latches Z9—Z13 Drawing	Latch
3.5		Display	Front Panel	120000, Blinking "1"		Display Drawing SH1	Display
3.6	DC V Mode	Sign	Front Panel Display	"+"		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.7	AC V Mode	Sign	Display	No Sign		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.8	kΩ Mode	Sign	Display	No Sign		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.9	No Range Activate	Impedance	Rear Panel Range Tabs 6, 11, T, B, H	Open Ckt		Auto Range Drawing SH2	x 10^4 Range
3.10	a) x .1 b) x 1 c) x 10 d) x 100 e) x 1K f) x 10K	Display, Relays	Display, Range Relays	Correct Decimal Point Relay per Table		Relay Table Drawing SH2	Decimal Point Display Relay Operation
3.11	Auto Range a) DC V b) kΩ c) Jump Z2 pin 8 to Z3 pin 8	Decimal Point Decimal Point Value	Display	Decimal Point a) x 1K b) x 10K c) "0" x .1		Auto Ranging Drawing SH2	Auto Range

Tests 4 and 5. See Figure 5-3

TEST NO	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
4.1		DC Volts	Z33 pin 8	+15V ✓	±1V Ripple 1mV RMS	Power Supply Drawing SH5	Analog Power Supply
4.2		DC Volts	Z33 pin 4	−15V ✓	±1V Ripple 1mV RMS	Power Supply Drawing SH5	Analog Power Supply
4.3		DC Volts	Z31A pin 7	−5V ✓	±1V Noise 25 μV	Power Supply Drawing SH5	Analog Power Supply
5	Short E62 to J21 J2 Jumper Z32A pin 6 to pin 7						Zero Input to A/D No EOC at End of Phase 3
5.1		Waveform	Z31A pin 5	Positive Pulses 100 msec		A/D Conv. Drawing SH4	Trigger & 10 Carry Start and End Phase 2
5.2	Select x.1 DCV	DC Volts	Amp A1 pin 5	<200 mV	+0, −	A/D Conv. Drawing SH4	A1 Operation OFF SET
5.3		DC Volts	Junction R96, R99	0V	±1V	A/D Conv. Drawing SH4	A2 and Clamp Circuits

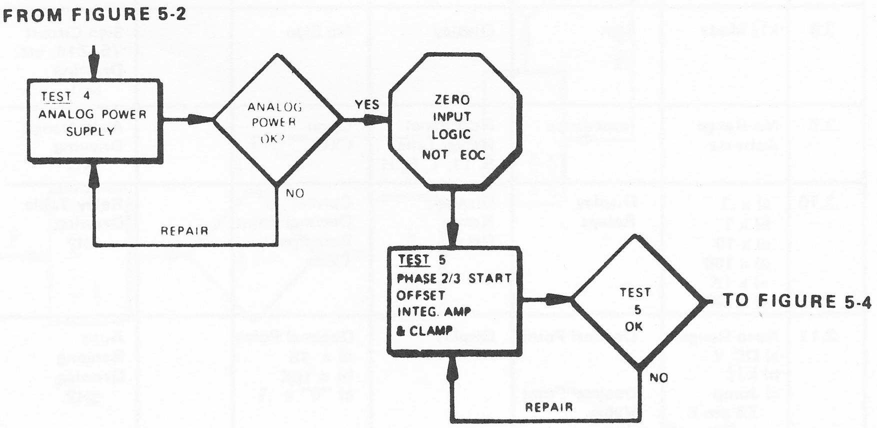

FROM FIGURE 5-2
TEST 4
ANALOG POWER SUPPLY
ANALOG POWER OK?
YES
NO
REPAIR
ZERO INPUT LOGIC NOT EOC
TEST 5
PHASE 2/3 START
OFFSET
INTEG. AMP
& CLAMP
TEST 5 OK
TO FIGURE 5-4
NO
REPAIR

Figure 5-3 Trouble Shooting Sequence Tests 4 and 5

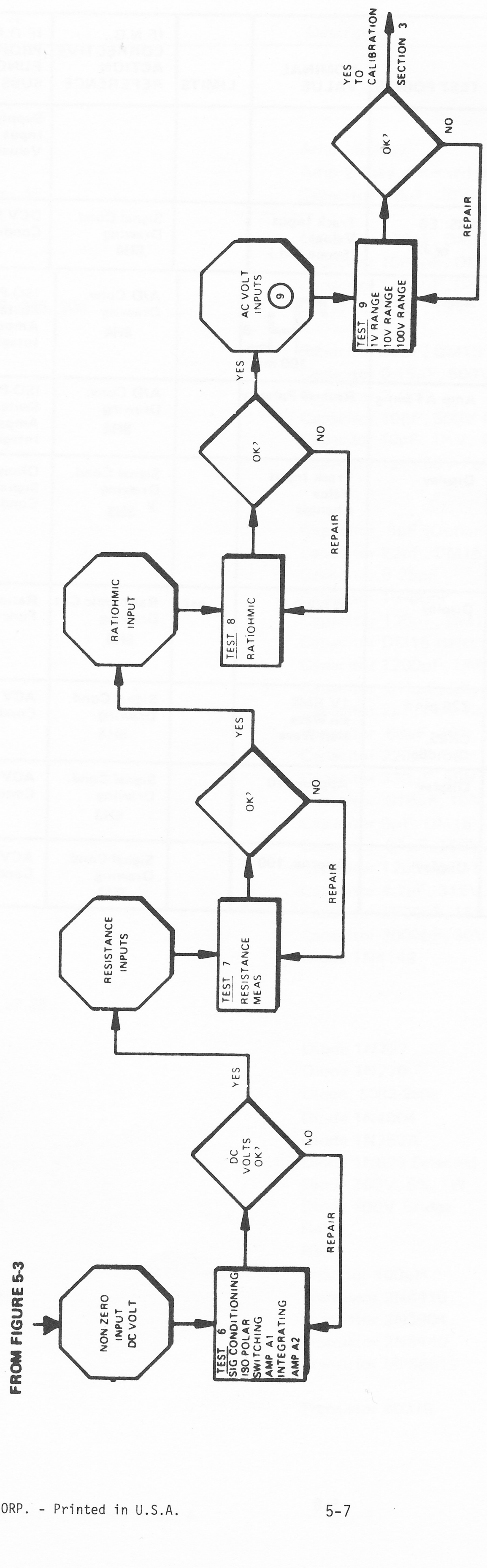
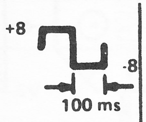

FROM FIGURE 5-3
NON ZERO INPUT DC VOLT
TEST 6
SIG CONDITIONING
ISO POLAR
SWITCHING
AMP A1
INTEGRATING
AMP A2
DC VOLTS OK?
NO
REPAIR
YES
RESISTANCE INPUTS
TEST 7
RESISTANCE MEAS
OK?
NO
REPAIR
YES
RATIOHMIC INPUT
TEST 8
RATIOHMIC
OK?
NO
REPAIR
YES
AC VOLT INPUTS
9
TEST 9
1V RANGE
10V RANGE
100V RANGE
OK?
NO
REPAIR
YES
TO CALIBRATION
SECTION 3

Figure 5-4 Trouble Shooting Sequence. Tests 6,7,and 8

Tests 6, 7, 8, and 9. See Figure 5-4.

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
6	Remove Short Connect Varying Vx DCV ±11V						Supply Varying Input Voltage Values
6.1	DCV Mode Range x 10	DC Volts	E35: E6 or J2	Track Input Values (Scope Ind.)		Signal Cond. Drawing SH4	DCV Signal Conditioning
6.2	+10V to Vx Sync. Scope to Z31 pin 5	Waveform	Amp A1 pin 5			A/D Conv. Drawing SH4	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
6.3	Reverse Input Vx Polarity	Waveform	Amp A1 pin 5	Reverse Polarity		A/D Conv. Drawing SH4	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
7	Connect for Resistance 2-Wire Connect Resistances in each Range kΩ Mode	Resistance Measurement	Display	Track Input Value Changes		Signal Cond. Drawing 3! SH3	Ohms Converter Signal Conditioning
8	Apply +10V to Both Vx and Rx RATIO Mode 10V Range	Display Count	Display	10.0000	± .010	Ratiohmic Ckt Drawing SH3	Ratiohmic Function
9.1	ACV Mode Range x 1 Apply -1V 200 Hz	Waveform	Z26 pin 6 CR25, Cathode	1V RMS sin Wave Half-Wave		Signal Cond. Drawing SH3	ACV Signal Conditioning
9.2	x 10 Range Apply 10 VRMS 200 Hz	Display Count	Display	Approx. 10		Signal Cond. Drawing SH3	ACV Signal Conditioning
9.3	x 100 Range	Display Count	Display	Approx. 100		Signal Cond. Drawing SH3	ACV Signal Conditioning

MAIN ASSEMBLY

Symbol	Description	Part No.
A1	Amp 1B Assy	PL30-1052(B37-1021)
A2	Amp 2 Assy, Selected per Dwg 32-3006	PL30-1001 (B37-1001)
C1, 18, 19, 39 thru 43	Capacitor 6.8µF, 20V	23-441005
C39 thru C43		
C2, C75	Capacitor 270pF, DM15	23-311022
C3, 5, 58	Capacitor 1000pF, DM15	23-111005
C4	Capacitor 1500pF, DM15	23-311038
C6, 24, 36, 44, 48, 205, 206	Capacitor 15µF, 10V	23-441003
C7	Capacitor 30pF, DM15	23-111004
C8	Capacitor 0.15µF, 600V, Poly C	23-510021
C9, 27	Capacitor 2-9pF	23-810006
C10	Capacitor 10pF, 500V DM15	23-311001
C11	Capacitor 10pF, 1KV, 10%, Selected	23-110003-A
C12, 25, 26	Capacitor 1µF, 50V Poly C	23-510001
C20, 23	Capacitor, 5pF (Optional FSV)	23-111003
C21, 22	Capacitor 82pF, DM15	23-111008
C28	Capacitor 6-25pF	23-810007
C30	Capacitor 15-60pF	23-810005
C29	Capacitor 120pF, DM15	23-310025
C31	Capacitor DM15 (select)	FSV
C32	Capacitor 1200pF, DM15	23-311037
C33	Capacitor .015µF, 2%, Poly Sty	23-550101
C34	Capacitor 2µF, Poly Carb	23-510002
C35	Capacitor .68µF, 10%, 50V	23-550104
C37, 203	Capacitor 220µF, 35V	23-620006
C38	Capacitor 330µF, 50V	23-620007
C45	Capacitor .018µF, 10%, 50V	23-550105
C46, 50	Capacitor 5pF, DM15	23-111003
C47	Capacitor .01µF, 150V, Disk	23-111006
C49	Capacitor 12pF, DM15	23-111002
C52	Capacitor 4.7µF, 315V, Alum	23-620004
C204	Capacitor 2500µF, 16V	23-620005
C300	Capacitor 3000pF, 30V	23-550103
CR2, 3, 4, 5	Diode 1N4148	24-110001
CR7 thru CR20		
CR22 thru CR24,27,28		
CR29, 36, 44		
CR6	Diode 1N702	24-120002
CR21	Diode 1N270	24-140270
CR25, 26	Diode, 5082-2800	24-110004
CR30 thru CR34	Diode 1N4004	24-104004
CR35, 213	Diode 1N752A	24-120075
CR37	Diode 1N829 Selected	24-130004
CR38	Diode 180V, 5%, 1W	24-121008
CR201, 202, 203	Diode 400V Bridge	24-100021
K1, K2	Relay	25-171002
K3 thru K6	Relay	25-171003
L1	Inductor 100µH	25-100024
Q1, 2, Q4 thru Q9	Transistor 2N4410	24-234410
Q3	Transistor 2N3904	24-233904
Q10	Transistor 2N3440	24-203440
Q16	Transistor MPS6519	24-246519
Q18, 20	Transistor 40319	24-220319

MAIN ASSEMBLY (Cont.)

Symbol	Description	Part No.
Q19	Transistor 40314	24–220314
Q22, 23	Transistor FET (Blue Dot)	24-48-1014-02
Q24, 25	Transistor FET (Yel Dot)	24-48-1014-05
Q27, 29, 30	Transistor FET (Orn Dot)	24-48-1014-10
Q40	Transistor 2N6027	24–206027
Q201	Transistor 2N5296	24–225296
R1, 8, 9, 10 R24 thru R28, 98, 109, 118, 121	Resistor 2.2K 5%, 1/4W, C. C.	22–022229
R2 thru R7, R122	Resistor 510K, 5%, 1/4W, C. C.	22–025149
R11	Resistor 11K, 5%, 1/4W, C. C.	22–021139
R12	Resistor 22K, 5%, 1/4W, C. C.	22–022239
R13, 17, 100, 101	Resistor 680Ω, 5%, 1/4W, C. C.	22–026819
R14, 18, 20, 22	Resistor 1.5K 5%, 1/4W, C. C.	22–021529
R15, 92	Resistor 33K 5%, 1/4W, C. C.	22–023339
R16	Resistor 100Ω, 5%, 1/4W, C. C.	22-021019-C
R19, 21, 23, 107	Resistor 3.3K, 5%, 1/4W, C. C.	22–023329
R29	Resistor Set Item 1 (6.429K)*	22-38-1006
R30, 38, 45, 300	Trimmer 25K	22–666253
R31	Resistor 162K, 1%, RN60C	22–371623
R32, 75, 87	Trimmer 250Ω	22–666251
R33	Resistor Set Item 2 (61.875K)*	22-38-1006
R34, 73, 78	Trimmer 2.5K	22–666252
R35	Resistor Set Item 3 (618.75K)*	22-38-1006
R36, 43, 51	Trimmer 500Ω	22–666501
R37, 52	Resistor Set Item 1 (89.75K, 0.1%)*	22-38-1007-3
R39	Resistor 6.19M, 0.1% RN65E	22–433000
R40, 53	Resistor Set Item 2 (10K, 0.1%)*	22-38-1007-3
R42	Resistor Set Item 1 (9.9M, 0.1%)*	22-38-1008-2
R44	Resistor Set Item 2 (99.75K, 0.1%)*	22-38-1008-2
R46, 86	Trimmer, 100Ω	22–666101
R47, 48, 96	Resistor 15K, 1%, RN55D	22-331502
R49, 97, 110, 119	Resistor 1K%, 1/4W, C. C.	22-021029-C
R50	Resistor 261K, 1%, RN60D	22-362613
R54	Resistor Set Item 1 (1 Meg)*	22-38-1008-1
R131, 132	Resistor 10Ω,5%, 1/8W, C.C.	22-011009
R58	Resistor 8.2M, 5%, 1/4W. C. C.	22–028259
R59, 83	Trimmer 100K	22–666104
R60, 95	Resistor 150K, 1%, RN55D	22-331503
R61	Resistor Set Item 6, (1.69K)*	22-38-1008-1
R62, 63, 74	Resistor Set Item 4 (10K)*	22-38-1008-1
R64	Resistor 100Ω 1%, RN60D	22-361000
R65, 66	Resistor Set Item 7 (2.49K)*	22-38-1008-1
R67	Resistor Set Item 8 (301K)*	22-38-1008-1
R68	Resistor Set Item 9 (178K)*	22-38-1008-1
R69	Trimmer 5K	22–666502
R70, 79	Resistor 100K, 5%, 1/4, C. C.	22–021049
R71	Resistor Set Item 2 (1 Meg)*	22-38-1008-1
R72	Resistor Set Item 3 (110K)*	22-38-1008-1
R76	Resistor Set Item 5 (1.1K)*	22-38-1008-1
R77, 106	Resistor 10K, 1%, RN55C	22-341002
R80	Resistor 47M 5%, 1/4W. C. C.	22–024769
R81	Resistor Set Item 2 (10.096K)*	22-38-1007-1
R82	Resistor 1M, 1%, RN65C	22-392001
R84	Resistor Set Item 1 (42K)*	22-38-1007-1
R85	Resistor Set Item 4 (37.95K)*	22-38-1007-1

***Must be ordered as part of designated set.**

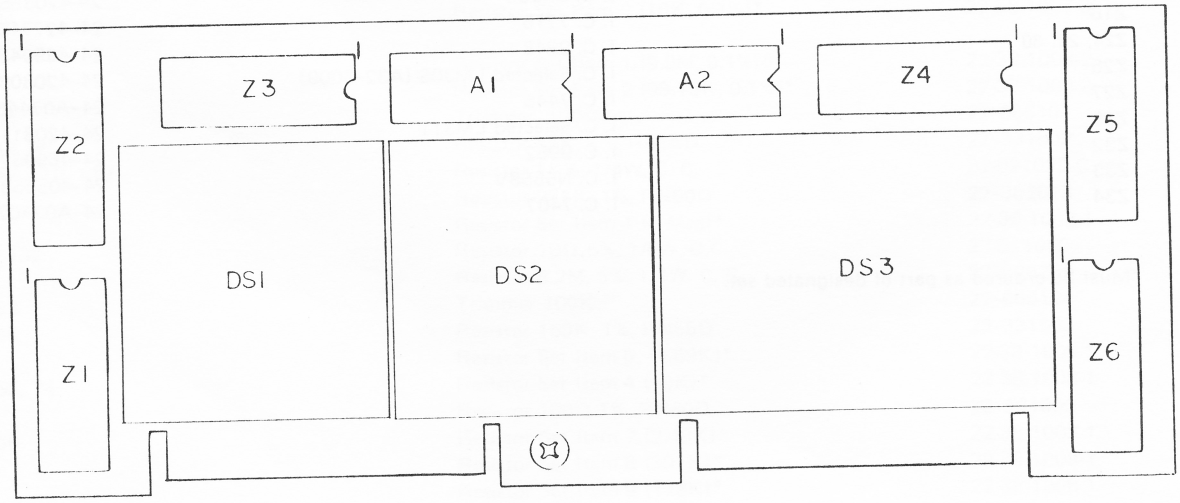
MAIN ASSEMBLY (Cont.)

Symbol	Description	Part No.
R88	Resistor RN55E	FSV
R89	Resistor Set Item 3 (10K)*	22-38-1007-1
R90	Resistor Set Item 2 (10K, 0.01%)*	22-38-1007-2
R91	Resistor Set Item 1 (52K, 0.01%)*	22-38-1007-2
R99	Resistor 3.01K, 1%, RN55D	22-333011
R102	Resistor 1.1K, 1% RN60C	22-371101
R103	Resistor 8.66K, 1%, RN55C	22-348661
R104	Resistor 10.5K, 1%, RN55D	22-331052
R105	Resistor 6.19K 1%, RN55C	22-346191
R108	Resistor 100Ω, 5%, 1/2W. C. C.	22-031019
R111	Resistor 10K 5%, 1/4W. C. C.	22-021039-C
R114	Resistor 47K, 10%, 1/4W. C. C.	22-024739
R120	Resistor 1M 5% 1/4W. C. C.	22-021059
R123	Resistor 47M, 5%, 1/4W. (Opt. FSV)	22-024769
R130	Resistor 3.6K, 5%, 1/4W. C. C.	22-023629
R201	Resistor 1K 5% 1/2W. C. C.	22-031029
R301	Resistor 82K 5% 1/4W. C. C.	22-028239
S1-S7	Switch	B38-1010
T1	Transformer	D36-1094
T2 thru T5	Transformer, Pulse	C36-1056
U1	Switch Module Assy	PL30-1003 (B37-1003)
Y1	Crystal 1MHZ	A38-1012
Z1, 28	I. C. 9937	24-469937
Z2, 20, 22, 31	I. C. 9094	24-469094
Z3, 21	I. C. 9949	24-469949
Z4 thru Z8	I.C. 7490	24-A07490
Z9 thru Z14	I. C. 7475	24-A07475
Z15	I. C. LF356	24-420356
Z16	I. C. 7715	24-427715
Z24, 26, 30	I. C. 9948	24-469948
Z25	I. C. Selected LM308 (A32-3009)	24-420308
Z27	I. C. 7445	24-A07445
Z29	I. C. Selected LM311	24-420311-01
Z32	I. C. 9962	24-469962
Z33	I. C. N5558V	24-405558
Z34	I. C. 7407	24-A07407

*Must be ordered as part of designated set.

DISPLAY ASSEMBLY

Symbol	Description	Part No.
A1	Res. Network, 2.2K, 14-Pin DIP	22-701002
A2	Res. Network, 15K, 14-Pin DIP	22-701000
DS1	Display	25-210351
DS2	Display	25-210352
DS3	Display	25-210353
Z1 thru Z6	I. C. DM8880	24-A08880


Z3
A1
A2
Z4
Z2
Z5
DS1
DS2
DS3
Z1
Z6

Chapter 6

REFERENCE SCHEMATICS

Figure 6-1 Signal Conditioning Schematic Dwg 35-1027 Sheet 3 (SH3)

Figure 6-2 A/D Converter Schematic Dwg 35-1027 Sheet 4 (SH4)

Figure 6-3 Counter and Display Schematic Dwg 35 1027 Sheet 1 (SH1)

Figure 6-4 Ranging Schematic Dwg 35-1027 Sheet 2 (SH2)

Figure 6-5 Power Supply Schematic Dwg 35-1027 Sheet 5 (SH5)

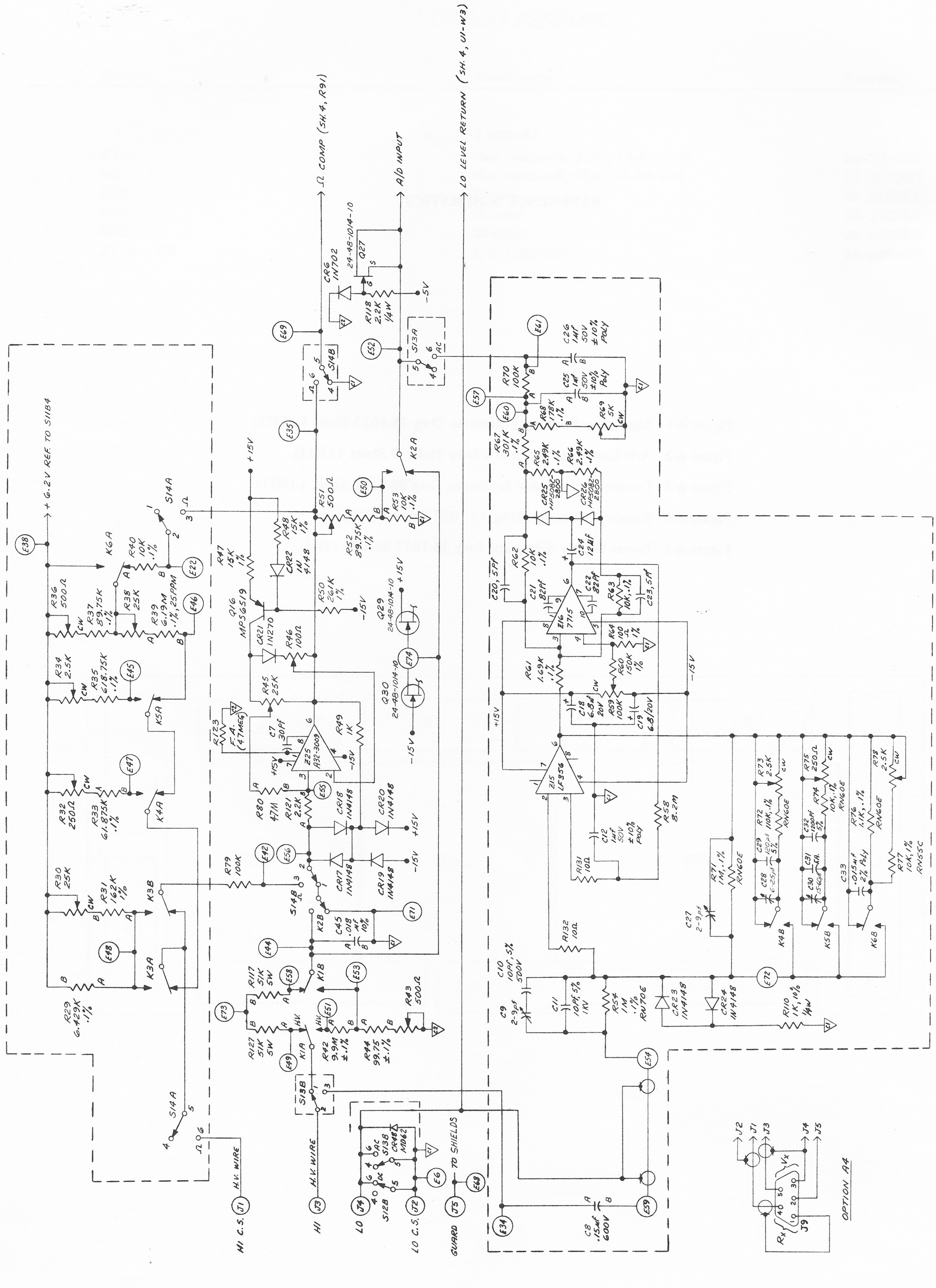

Ω COMP (SH.4, R91)
A/D INPUT
LO LEVEL RETURN (SH.4, U1-W3)
+6.2V REF. TO S11B4
HI C.S. J1
H.V. WIRE
HI J3
H.V. WIRE
LO J4
LO C.S. J2
GUARD J5
TO SHIELDS
Z15 LF356
Z16 7715
Z25 A32-3009
Q16 MPS6519
Q27 24-48-1014-10
Q29 24-48-1014-10
Q30 24-48-1014-10
S13A
S13B
S14A
S14B
S12B
E38
E22
E46
E45
E47
E48
E42
E56
E55
E44
E58
E53
E51
E73
E49
E71
E74
E50
E35
E69
E52
E57
E60
E61
E72
E54
E59
E34
E6
E68
J2
J1
J3
J4
J5
J9
Rx
Vx
OPTION A4

Figure 6-1 Signal Conditioning Schematic Dwg 35-1027 Sheet 3

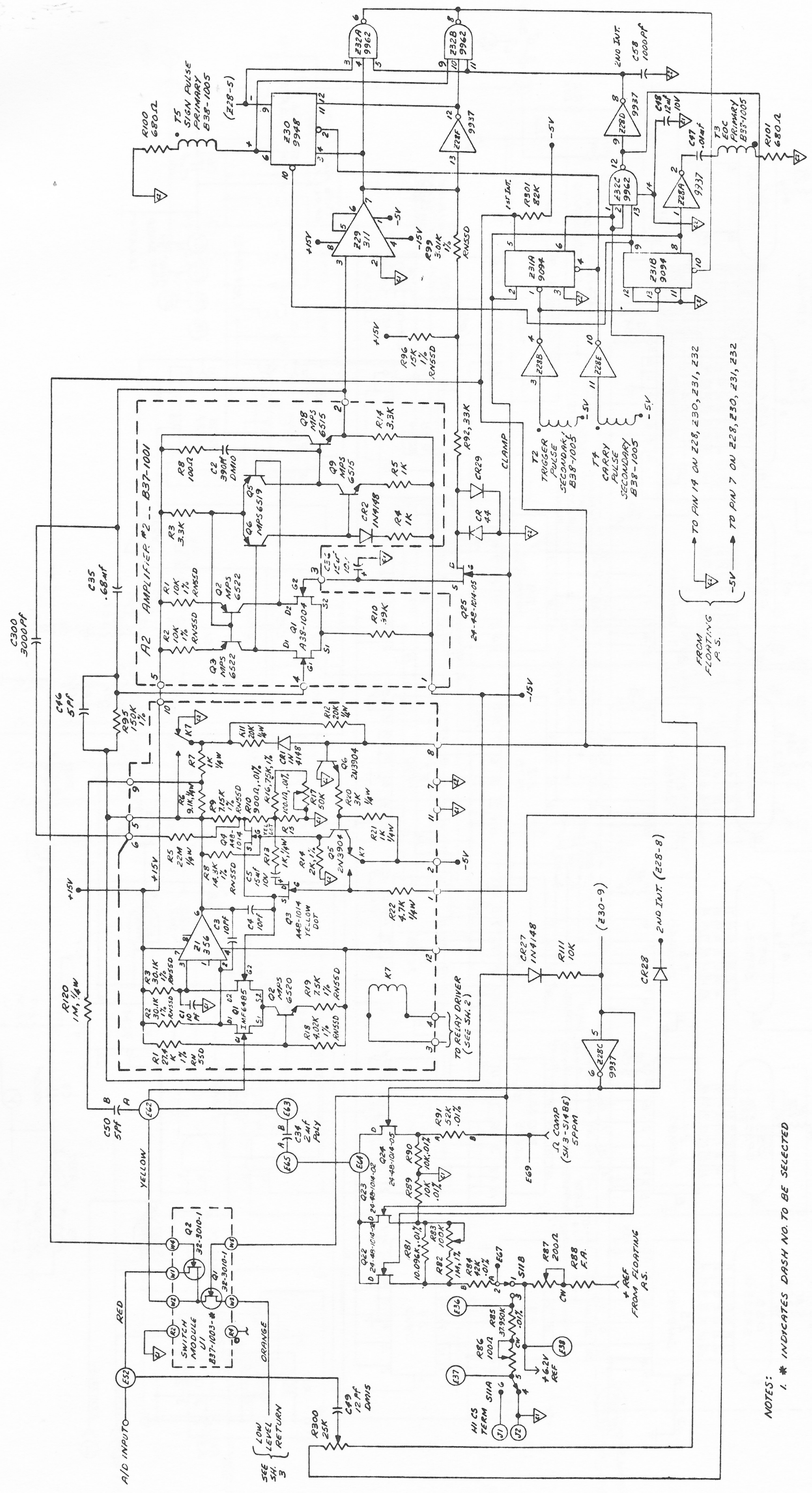

R100 680Ω
T5 SIGN PULSE PRIMARY B38-1005
(Z28-5)
Z30 9948
Z32A 9962
Z32B 9962
Z28F 9937
2ND INT.
C58 1000pF
Z29 311
+15V
-15V
-5V
R99 3.01K 1% RN55D
R301 82K
1st INT.
Z32C 9962
Z28D 9937
C48 1.2µf 10V
C47 .01µf
T3 EOC PRIMARY B38-1005
R101 680Ω
Z28A 9937
Z31A 9094
Z31B 9094
R96 15K 1% RN55D
Z28B
Z28E
T2 TRIGGER PULSE SECONDARY B38-1005
T4 CARRY PULSE SECONDARY B38-1005
A2 AMPLIFIER #2 ... B37-1001
Q8 MPS 6515
R14 3.3K
Q9 MPS 6515
R8 100Ω
C2 390pf DM10
R92 33K
CR29
CLAMP
Q5 MPS6519
Q6 MPS6519
R5 1K
R4 1K
CR2 1N148
CR 44
R3 3.3K
R1 10K 1% RN55D
R2 10K 1% RN55D
Q2 MPS 6522
Q3 MPS 6522
Q1 A38-1004
Q25 24-48-1014-05
R10 39K
C35 .68µf
C300 3000pF
C46 5pF
R95 150K 1%
TO PIN 14 ON Z28, Z30, Z31, Z32
TO PIN 7 ON Z28, Z30, Z31, Z32
FROM FLOATING P.S.
R120 1M, 1/4W
K7
R7 1K 1/4W
R11 20K 1/4W
R12 20K 1/4W
CR1 1N4148
Q6 2N3904
R6 9.1K 1/4W
R9 7.15K 1% RN55D
R10 900Ω .01%
R16 .75K 1%
R17 50K
R20 3K 1/4W
R5 22M 1/4W
R8 14.3K 1% RN55D
Q4 A48-1014
R13 1K 1/4W
R14 2K 1%
Q5 2N3904
R21 1K 1/4W
C5 .15µf 10V
Q3 A48-1014 YELLOW DOT
R22 4.7K 1/4W
Z1 356
C3 10pf
C4 10pf
R23 301K 1% RN55D
R2 301K 1% RN55D
Q1 IMF6485
Q2 MPS 6520
R19 7.5K 1% RN55D
R18 4.02K 1% RN55D
R1 274K 1% RN55D
TO RELAY DRIVER (SEE SH. 2)
CR27 1N4148
R111 10K
(Z30-9)
2ND INT. (Z28-8)
CR28
Z28C 9937
C50 5pF
YELLOW
C34 2µf Poly
Ω COMP (SH 3-S11BE) 5PPM
R91 52K .01%
Q24 24-48-1014-05
R89 10K .01%
R90 10K .01%
Q23 24-48-1014-05
Q22 24-48-1014-05
R81 10.096K .01%
R83 10K 1%
R82 1M 1%
R84 42K .1%
S11B
R87 200Ω
R88 F.A.
+REF FROM FLOATING P.S.
R85 37.950K .01%
R86 100Ω
+6.2V REF
HI CS TERM S11A
Q2 32-3010-1
Q1 32-3010-1
SWITCH MODULE U1 B37-1003-*
RED
ORANGE
A/D INPUT
LOW LEVEL RETURN
SEE SH. 3
R300 25K
C49 12pf DM15
NOTES:
1. * INDICATES DASH NO. TO BE SELECTED

Figure 6-2 A/D Converter Schematic Dwg 35-1027 Sheet 4 (SH4)

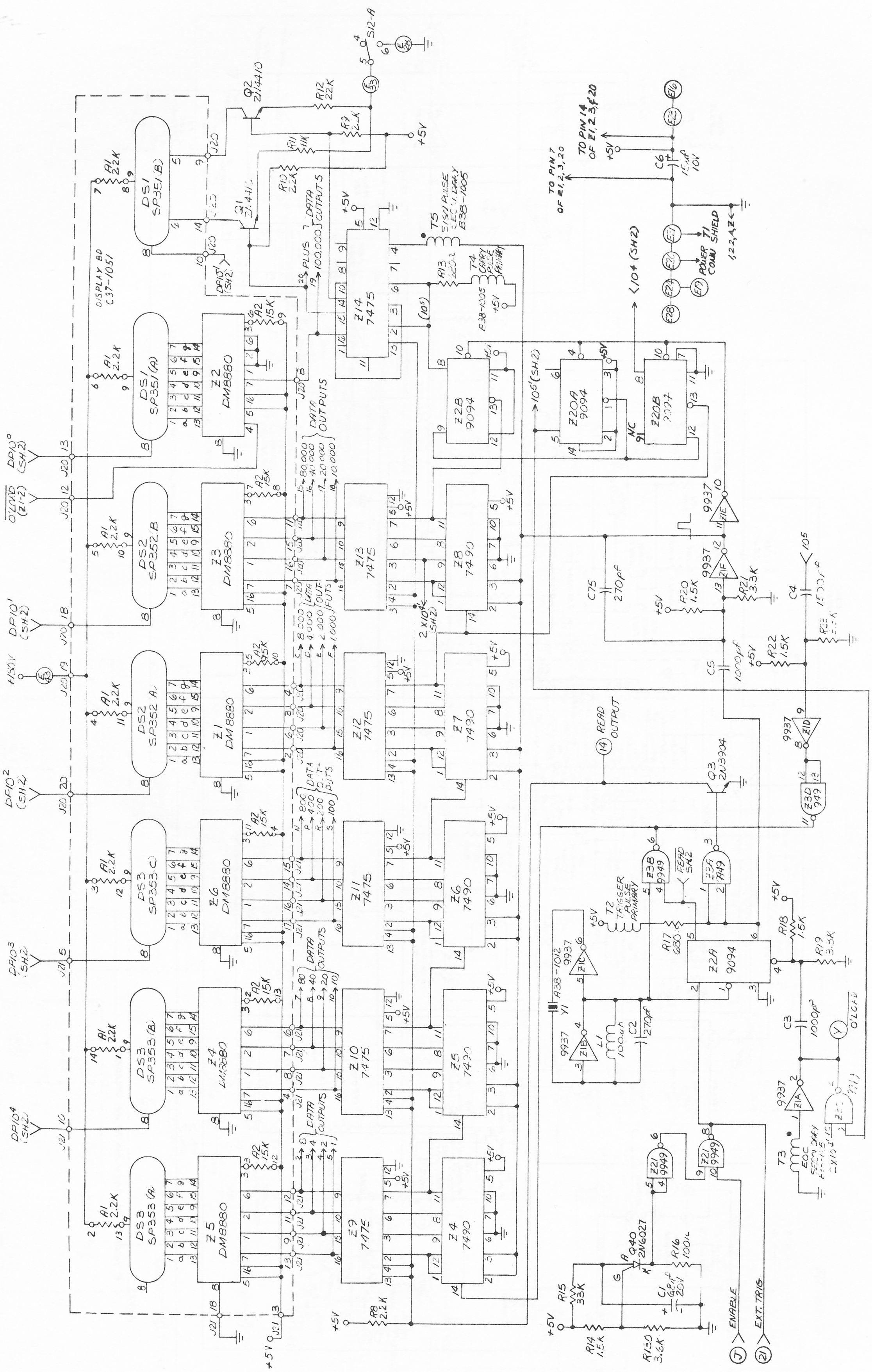
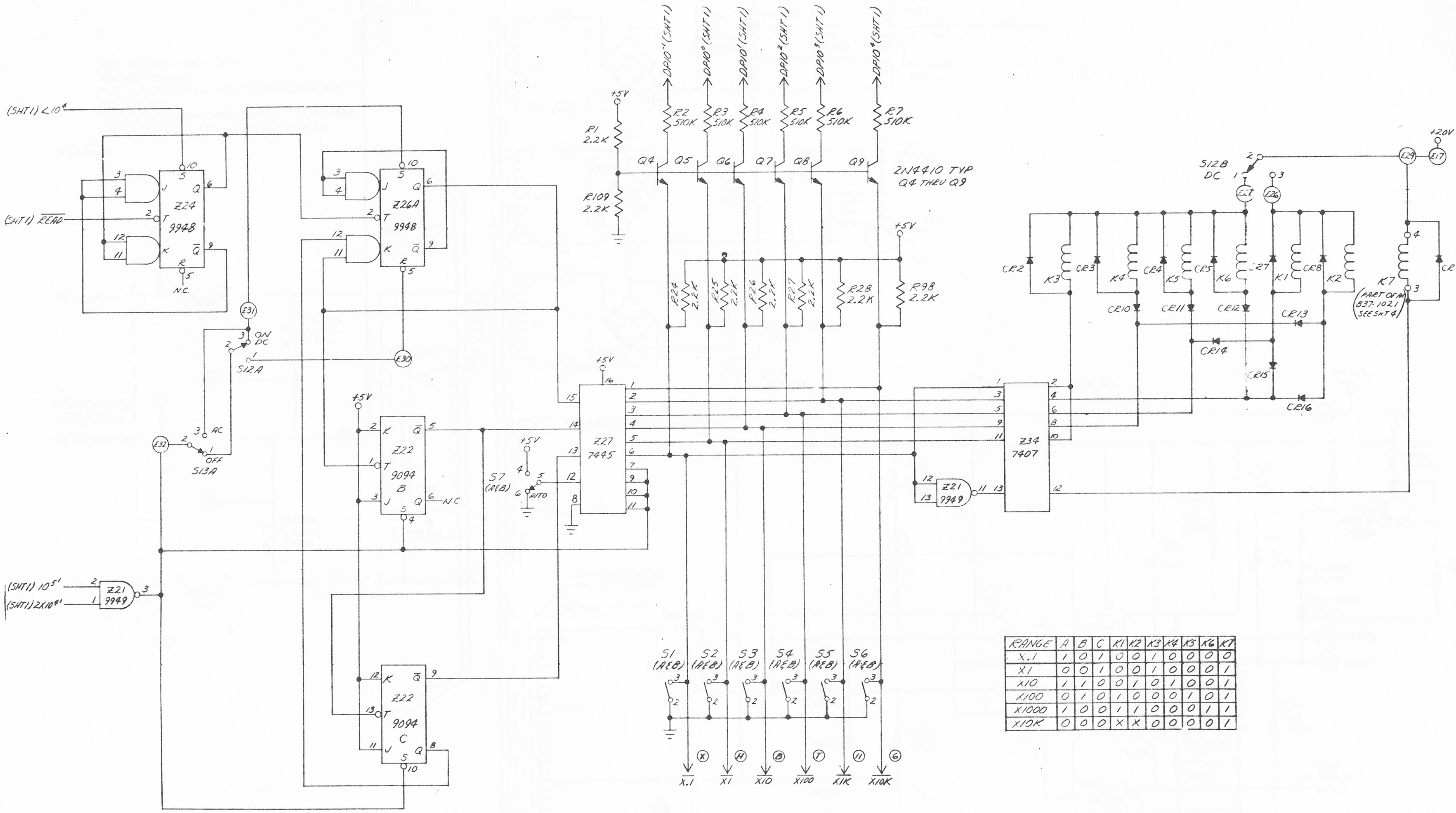

DISPLAY BD C37-1051
DS1 SP351(B)
DS1 SP351(A)
DS2 SP352 B
DS2 SP352 A
DS3 SP353 C
DS3 SP353 B
DS3 SP353 A
Z2 DM8880
Z3 DM8880
Z1 DM8880
Z6 DM8880
Z4 DM8880
Z5 DM8880
Z14 7475
Z13 7475
Z12 7475
Z11 7475
Z10 7475
Z9 7475
Z8 7490
Z7 7490
Z6 7490
Z5 7490
Z4 7490
Z2B 9094
Z20A 9094
Z20B 9094
Z2A 9094
Q1 2N4410
Q2 2N4410
Q3 2N3904
Q40 2N6027
R1 2.2K
R2 15K
R8 2.2K
R9 2.2K
R10 22K
R11 11K
R12 22K
R13 220Ω
R14 1.5K
R15 33K
R16 100Ω
R17 680
R18 1.5K
R19 3.3K
R20 1.5K
R21 3.3K
R22 1.5K
R150 3.6K
C1 68µF 20V
C2 270pF
C3 1000pF
C4 150pF
C5 1000pF
C6 15µF 10V
C75 270pF
L1 100µh
Y1 A38-1012
T2 TRIGGER PULSE PRIMARY
T3 EOC SEC'Y DRY
T4 CARRY PULSE PRIMARY
T5 SIGN PULSE SEC'Y DRY B38-1005
B38-1005
9937
9949
DATA OUTPUTS
PLUS 100,000
READ OUTPUT
OVLRD
ENABLE
EXT. TRIG
TO PIN 7 OF Z1,2,3,20
TO PIN 14 OF Z1,2,3,&20
POWER COMM SHIELD
S12-A
+5V
+190V
DP10° (SH2)
DP10¹ (SH2)
DP10² (SH2)
DP10³ (SH2)
DP10⁴ (SH2)
OVLRD (Z1-2)
2 X10⁴ (SH2)
10⁵ (SH2)
10⁵
10⁴ (SH2)
READ SH2
J20
J21

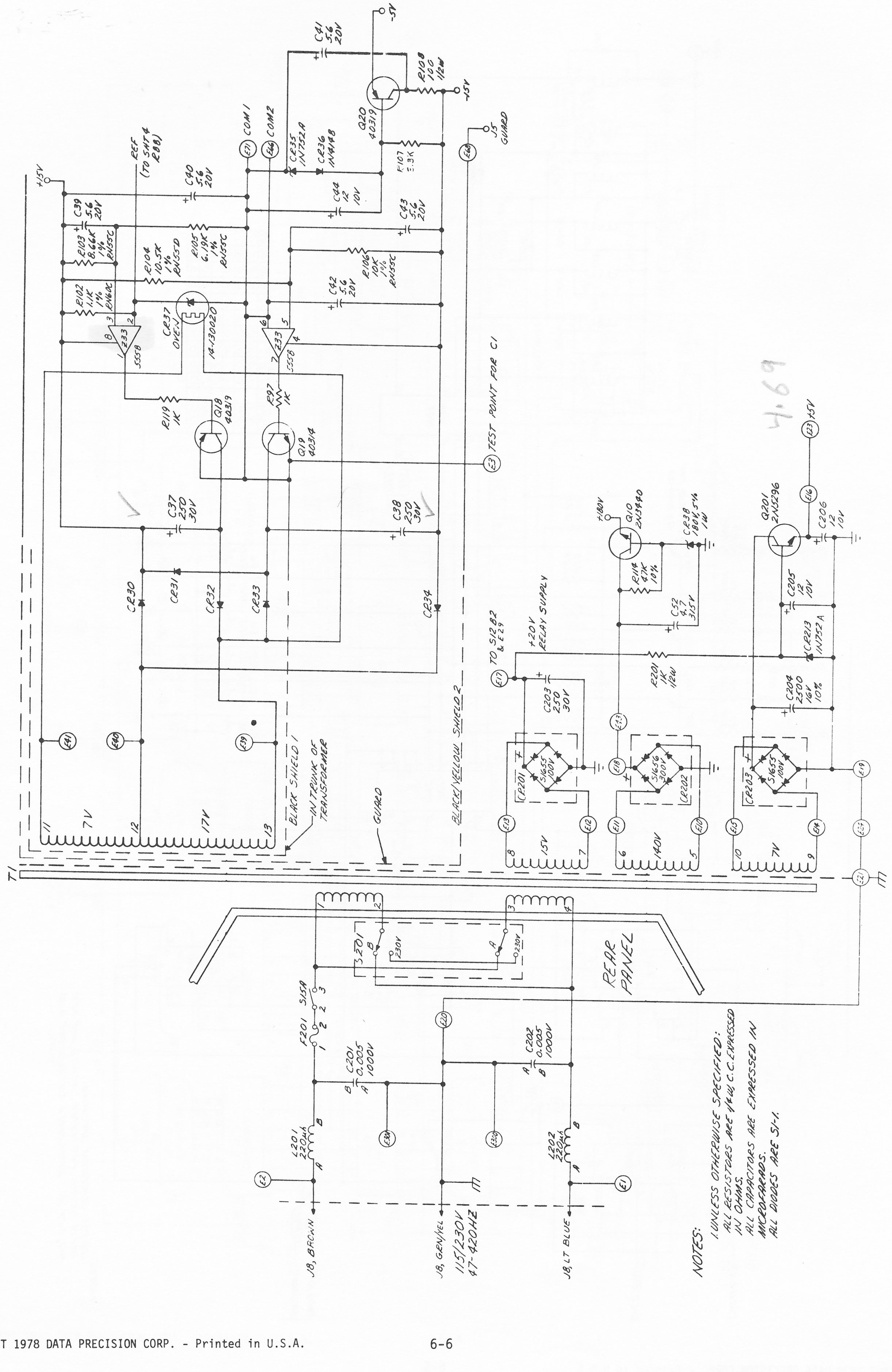
Figure 6-3 Counter and Display Schematic Dwg 35-1027 Sheet 1 (SH1)


(SHT1) <10⁴
(SHT1) READ
(SHT1) 10⁵'
(SHT1) 2X10⁴'
Z24 9948
Z26A 9948
Z22 9094 B
Z22 9094 C
Z21 9949
Z27 7445
Z34 7407
S12A ON DC
S13A AC OFF
S7 (REB) AUTO
S12B DC
E29
E17
E26
E27
E30
E31
E32
+5V
+20V
N.C.
P1 2.2K
R109 2.2K
R2 510K
R3 510K
R4 510K
R5 510K
R6 510K
R7 510K
R24 2.2K
R25 2.2K
R26 2.2K
R27 2.2K
R28 2.2K
R98 2.2K
Q4
Q5
Q6
Q7
Q8
Q9
2N4410 TYP Q4 THRU Q9
DP10⁻¹(SHT1)
DP10⁰(SHT1)
DP10¹(SHT1)
DP10²(SHT1)
DP10³(SHT1)
DP10⁴(SHT1)
K1
K2
K3
K4
K5
K6
K7 (PART OF AR 837-1021 SEE SHT 4)
CR2
CR3
CR4
CR5
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
S1 (REB)
S2 (REB)
S3 (REB)
S4 (REB)
S5 (REB)
S6 (REB)
X.1
X1
X10
X100
X1K
X10K

RANGE	A	B	C	K1	K2	K3	K4	K5	K6	K7
X.1	1	0	1	0	0	1	0	0	0	0
X1	0	0	1	0	0	1	0	0	0	1
X10	1	1	0	0	1	0	1	0	0	1
X100	0	1	0	1	0	0	0	1	0	1
X1000	1	0	0	1	1	0	0	0	1	1
X10K	0	0	0	X	X	0	0	0	0	1

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
PIN 14 OF ALL INTEGRATED CIRCUITS ARE +5V.
PIN 7 OF ALL INTEGRATED CIRCUITS ARE GND.

Figure 6-4 Ranging Schematic Dwg 35-1027 Sheet 2 (SH2)


+15V
REF (TO SHT 4 R88)
C39 5.6 20V
C40 5.6 20V
R103 8.66K 1% RN55C
R104 10.5K 1% RN55D
R105 6.19K 1% RN55C
R102 1.1K 1% RN60C
CR37 OVEN 14-130020
Z33 558
R106 10K 1% RN55C
C42 5.6 20V
C43 5.6 20V
C44 12 10V
CR35 1N752A
CR36 1N4148
E71 COM 1
E66 COM 2
Q20 40319
R107 3.3K
R108 100 1/2W
C41 5.6 20V
-5V
+5V
J5 GUARD
E68
R119 1K
Q18 40319
R97 1K
Q19 40314
E3 TEST POINT FOR C1
C37 250 30V
C38 250 30V
CR30
CR31
CR32
CR33
CR34
E41
E40
E39
11
7V
12
17V
13
BLACK SHIELD 1
IN TRUNK OF TRANSFORMER
GUARD
BLACK/YELLOW SHIELD 2
T1
E17 TO S1282 & E29
+20V RELAY SUPPLY
C203 250 30V
CR201 S1655 100V
E13
15V
E12
8
7
+180V
Q10 2N3440
CR38 180V 5% 1W
R114 47K 10%
C52 4.7 315V
R201 1K 1/2W
E18
CR202 S1656 300V
E11
140V
E10
6
5
Q201 2N5296
C206 12 10V
E16
E23 +5V
C205 12 10V
CR213 1N752A
C204 2500 16V 10%
CR203 S1655 100V
E19
E15
7V
E14
10
9
E37
E21
1
2
3
4
S201 B 230V
A 230V
REAR PANEL
F201 S1.5A
1 2 2 3
C201 0.005 1000V
B A
C202 0.005 1000V
A B
E20
E30
E36
L201 220μH
A B
L202 220μH
A B
E2
E1
J8, BROWN
J8, GRN/YEL
115/230V 47-420HZ
J8, LT BLUE
4.69

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W C.C. EXPRESSED IN OHMS.
ALL CAPACITORS ARE EXPRESSED IN MICROFARADS.
ALL DIODES ARE S1-1.

Figure 6-5 Power Supply Schematic Dwg 35-1027 Sheet 5 (SH5)

DATA PRECISION

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